

Exam solutions ASIC (TSTE81) 010316

1. a) The transformation of a representation from one design level to a lower abstraction level is called synthesis.
- b) In-place computing means that the inputs to the computation are not needed once the computation has started. The memory locations can therefore be used to store the result of the computation.
- c) No. One example of an addition with constant latency (independent of the number of bits to add) is the addition approach shown in Example 11.4 on page 468 in "DSP Integrated Circuits". Another example is the bit-serial adder.
- d) The transfer function of a pipelined digital filter will have the same attenuation as the original filter, but the group delay (the derivative of the phase) will be increased by a constant factor.
- e) A fully specified signal-flow graph is described in terms of operations that can be executed by the processing elements that are going to be used in the implementation. Example: Addition of 3 values when only 2 input additions are possible (see Figure 6.13 on page 234).

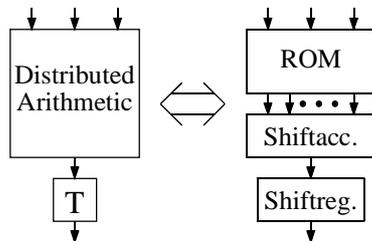
2. a)

$$v_1(n+1) = x(n) + av_1(n) + dv_2(n)$$

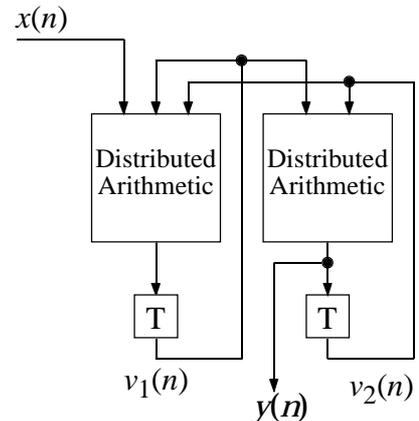
$$v_2(n+1) = bv_1(n) + cv_2(n)$$

$$y(n) = v_2(n+1)$$

The combination of a delay element and a distributed arithmetic unit really corresponds to:



and the single delay element corresponds to a shift register.

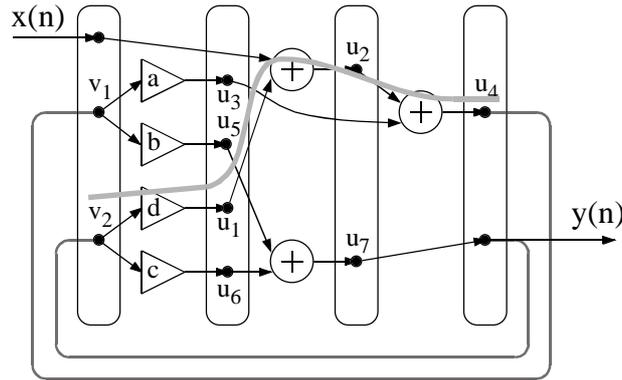


b) $y(n) = 1.125_{10}v_1(n) - 0.125_{10}v_2(n) = 01.001_{2C}v_1(n) + 11.111_{2C}v_2(n)$

$v_1(n)$ $v_2(n)$	$y(n)$
0 0	0 = 00.000
0 1	-0.125 = 11.111
1 0	1.125 = 01.001
1 1	1 = 01.000

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3. a)

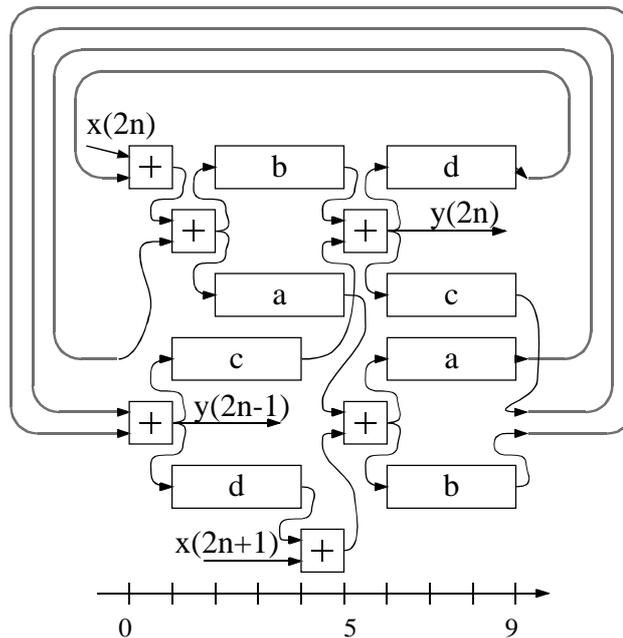


b) Critical path = longest computational path from input to output, from input to delay element, between two delay elements, or from one delay element to output. Longest computational path is from $v_2(n)$ to the first delay element $v_1(n)$. The critical path is $3+1+1 = 5$ time units long.

$$c) T_{\min} = \max (T_{\text{opi}}/N_i) = \max ((T_a+T_{\text{add}})/1, (T_c+T_{\text{add}})/1, (T_d+T_{\text{add}}+T_{\text{add}}+T_b+T_{\text{add}})/2) = \max ((3+1)/1, (3+1)/1, (3+1+1+3+1)/2) = \max (4, 4, 4.5) = 4.5 \text{ tidsenheter.}$$

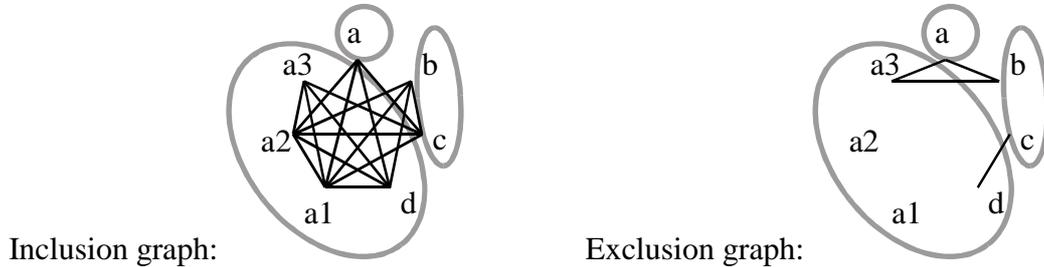
Minimum sample period is 4.5 time units.

d) T_{\min} is a fractional number of time units. Must therefore schedule of two sample periods.

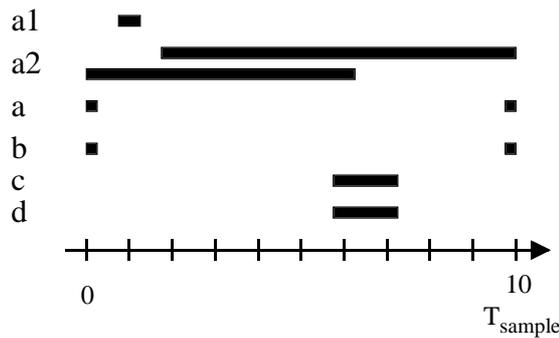


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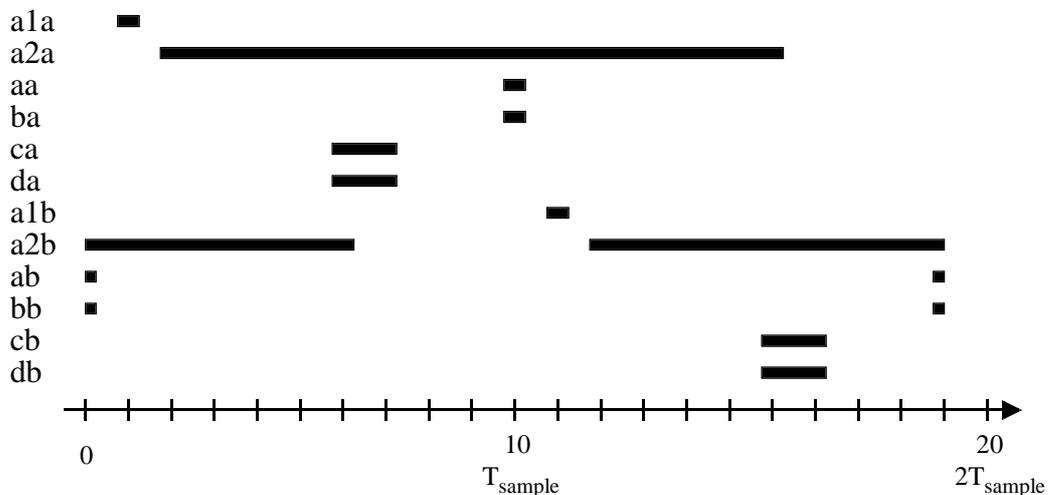
4. a) Name additions A1 to A3 from left in the figure. Draw an inclusion graph (connect nodes where the corresponding operations can share a resource). Find the minimum number of cliques (fully connected subgraphs). This can be difficult as there are a lot of edges in the graph. An alternative solution is to use an exclusion graph, where an edge defines that the connected operations can not share a resource.



b) Extract variable lifetimes. The name of a variable is the same as the operation that generates the variable. Direct communication between processing elements may be available (depends on the selected architecture). Assume that all communication has to go through the memory.

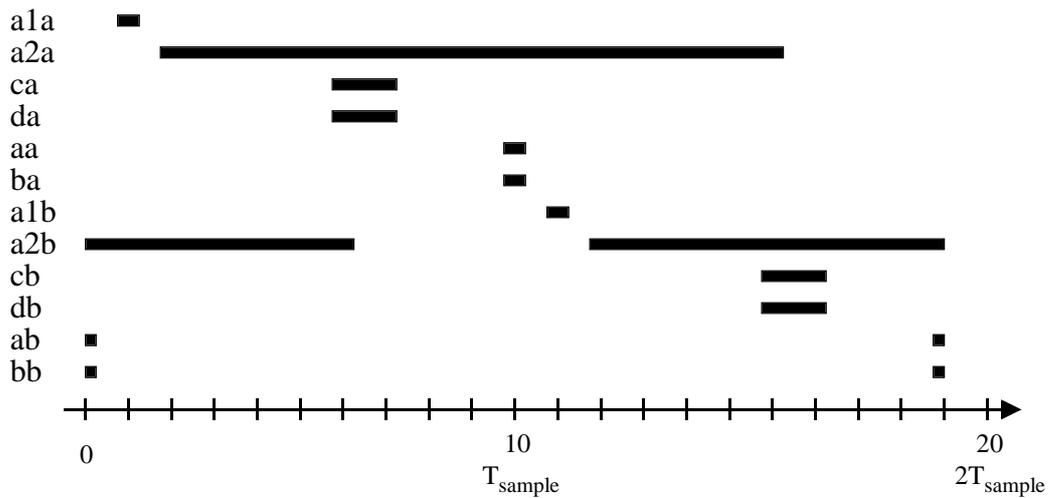


Note that there are variables that lives longer than a single sample period. Must therefore draw a lifetime diagram for two sample periods. Add a and b to the names to indicate first or second sample period.

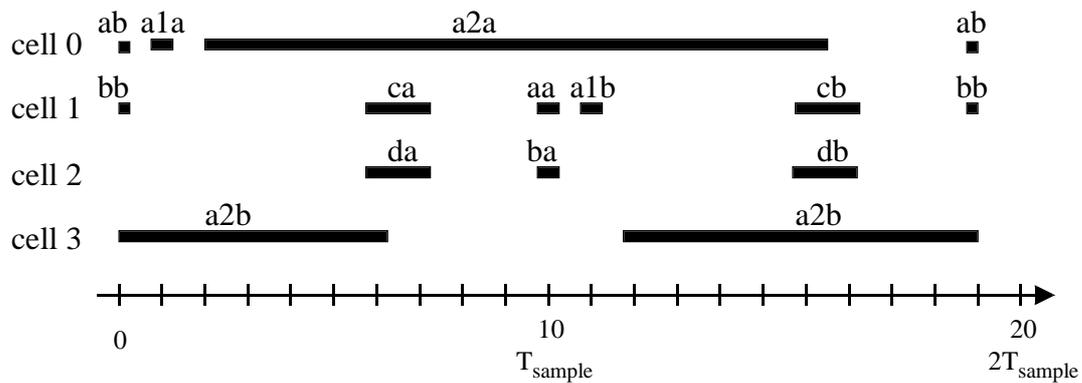


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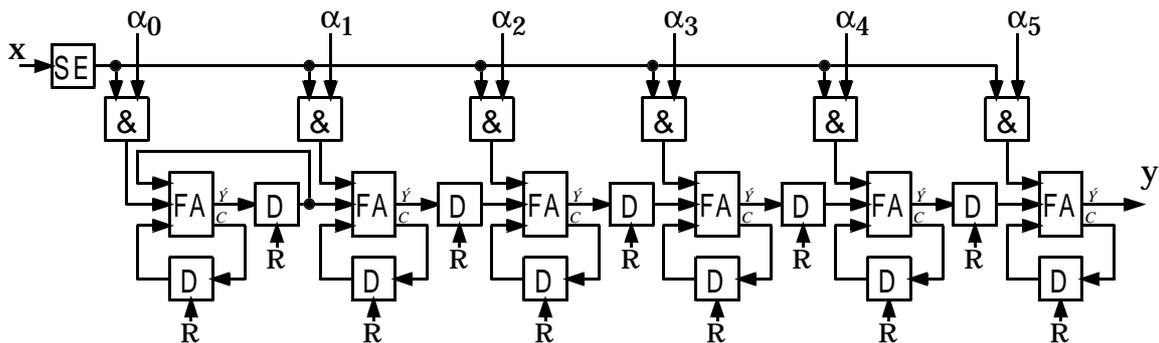
Left edge: Sort variables according to starttime and length.



Allocate one memory cell and assign variables by traversing the list from beginning. Allocate cells until every variable in the list has been assigned to a memory cell.



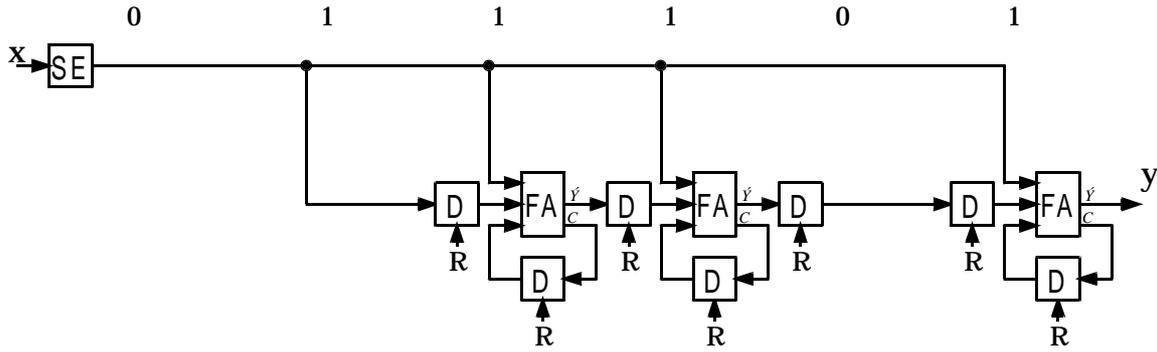
5. a)



The structure is reset at the start of the calculation using the signal R. The block SE is extending the sign by copying the sign bit. It is also possible to replace the first step with a subtraction of x times a_0 . The feedback of the first bitslice would then be removed, and the carry flipflop should be set instead of reset at the start of the multiplication.

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b) $0.90625_{10} = 0.11101_{2C}$.



c) $0.11101_{2C} = 1.00-101_{CSDC}$. Note that the initial 1 is not of weight -1 but of weight 1 .

(Compare with 2's complement where the sign bit has a weight of -1). The S control signal is setting the value of the flipflop to 1 at the start of the calculation. Another equally correct solution would be to use $0.11101_{2C} = 1.000-1-1_{SDC}$.

