Linköping Institute of Technology
Department of Electrical Engineering, Integrated Circuits and Systems

Exam TEN1 in TSTE85 Low Power Electronics

Time:	Friday 31 Augusti 2018, 8:00–12:00
Place:	TER1
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aids:	Calculator and appended formula page
Instructions:	Maximum score is 70 p and minimum score to pass is 30 p
Solutions:	Posted on the course web page
Grades:	Posted through LADOK by Tuesday 18 September 2018
Display:	Time and place will be posted with the grades

1.

a) Give examples on historical applications that have been driving forces in the field of low power electronics. (2 p)

b) What is clock gating and how can it be used to reduce power consumption? (2 p)

c) A phase-locked loop (PLL) is a power hungry component that is used to implement the local oscillator in radios. Explain the technique of duty cycling the PLL in order to reduce the transmitter power consumption. (2 p)

d) What are the advantages of using asynchronous techniques in a digital circuit operating in subthreshold mode? (2 p)

e) Consider an adiabatic circuit for which the power clock is high. Explain how a fast transition on the input affects the energy dissipation. (2 p)

2. The NMOSFET in the CMOS inverter shown in Figure 1 draws the subthreshold current $0.5e^{-25|V_{GT}|}$ µA from the supply at room temperature when V_{DD} = 1 V, V_{in} = 0 V, V_{SBn} = 0 V, and V_{Tn} = 0.3 V. Neglect channel length modulation in calculations.

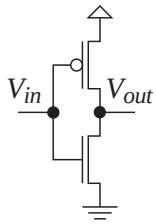

Figure 1. CMOS inverter.

a) What is the subthreshold slope *S* of the NMOSFET? (4 p)

b) How much relative power would be saved if V_{Tn} could be increased to 0.4 V? (4 p)

c) Suggest a method to increase V_{Tn}. (2 p)

3. Consider the design of an *n*-bit up-counter where *n* is large. Compare the average number of transitions in a binary-coded counter with a Gray-coded counter. (6 p)

4. In the full adder shown in Figure 2, the carry bit is generated by the function $f_j = a_j b_j + c_j(a_j \oplus b_j)$. The inputs to the full adder are uncorrelated and glitch free with probablities $P(a_j=1) = 0.5$, $P(b_j=1) = 0.5$, and $P(c_j=1) = 0.25$.

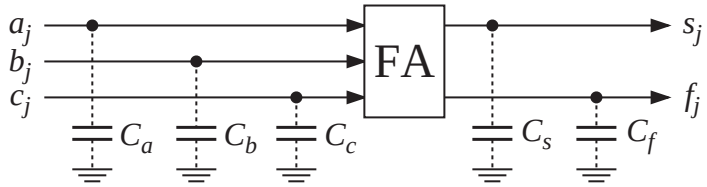

Figure 2. Full adder with parasitic capacitances.

a) Determine the power consumption due to switching of the parasitic capacitances C_a, C_b, C_c, and C_f, assuming a power supply voltage of V_{DD}. (8 p)

b) How large is the power reduction if the power supply voltage is reduced by 15% and the clock frequency is reduced by 20%? (2 p)

5. An estimate of the minimum power consumption of a single-pole low-pass filter with bandwidth B is plotted in Figure 6 as a function of SNR for analog (normal line) and digital (dashed line) circuits.

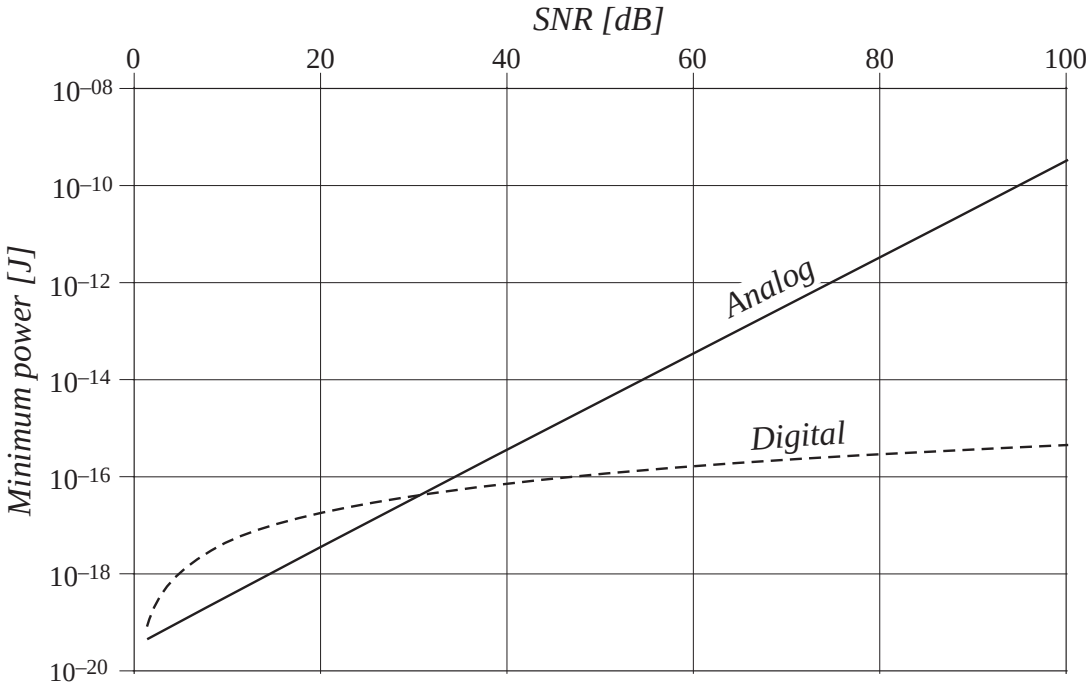

Figure 6. Minimum power consumption for analog and digital circuits.

a) What *fundamental limit* bounds the power consumption of the circuits? (2 p)

b) What *circuit limit* bounds the power consumption of the circuits? (2 p)

c) How many bits n are approximately needed in order for the digital circuit to be more power efficient than the analog circuit assuming SNR ≈ $6.0n$ + 1.8 dB? (2 p)

6. A circuit used for adding three 6-bit binary numbers $X = \langle x_5, \ldots, x_0 \rangle$, $Y = \langle y_5, \ldots, y_0 \rangle$, $Z = \langle z_5, \ldots, z_0 \rangle$ and computing a sum $S = \langle s_5, \ldots, s_0 \rangle$ is shown in Figure 3. The inputs come from registers. A full adder (FA) has the propagation delay 60 ps for all inputs to all outputs. To solve the problems below you may use 2:1 multiplexers that have a propagation delay of 50 ps, and inverters that have a propagation delay of 30 ps.

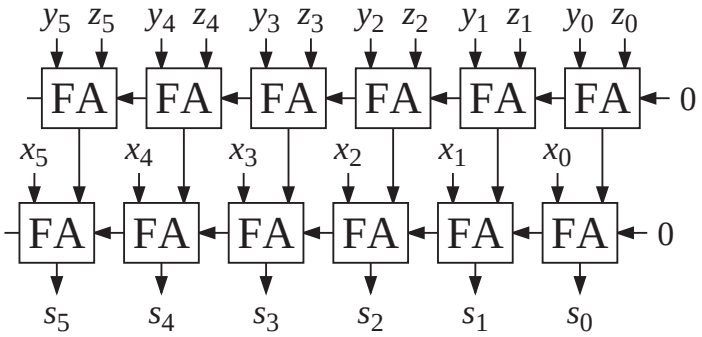

Figure 3. Adder circuit.

a) Explain why different delays in the paths to an FA consume extra power . (2 p)

b) Estimate how much power that could be saved by delay balancing the circuit. For simplicity, assume that the dynamic power dissipation of an inverter is 20% of the power of an FA. Further assume that the power dissipation of an FA doubles with every 100 ps difference in maximum skew at the inputs. (8 p)

c) Interleave the circuit with a factor of 2. How much power can be saved from voltage scaling if the original throughput is maintained? Assume V_{DD} = 1.0 V, V_t = 0.25 V and r = 1.5. Neglect capacitance from extra multiplexers and registers. (8 p)

7. Two unsigned three-bit binary numbers $A = \langle a_2 a_1 a_0 \rangle$ and $B = \langle b_2 b_1 b_0 \rangle$ should be compared as $f = A \geq B$. a_2 and b_2 are the MSBs, and a_0 and b_0 are the LSBs. A straightforward comparator can be designed by adding the two's complement value of B to A, and using the carry output from the MSB position as the result. Since we are not interested in the subtractor output, it is sufficient to only compute the carries, e.g. with the equations shown below.

$$c_0 = 1 \qquad \text{(1 LSB is added for two's complement)}$$

$$c_1 = a_0 \overline{b_0} + c_0 \left(a_0 + \overline{b_0} \right) \qquad \text{(inversions of } b_i \text{ are needed for one's complement)}$$

$$c_2 = a_1 \overline{b_1} + c_1 \left(a_1 + \overline{b_1} \right)$$

$$c_3 = a_2 \overline{b_2} + c_2 \left(a_2 + \overline{b_2} \right)$$

$$f = c_3$$

The task is to design a subset-disabling precomputed comparator.

a) Compute the Observability Don't Care set for $f = c_3(a_2, b_2, c_2)$ with respect to c_2. (5 p)

b) Use the Observability Don't Care set to realize the precomputed comparator. (5 p)

TSTE85 FORMULAS

Circuits

Transition activity $\alpha = \alpha_{01} + \alpha_{10} = 2\alpha_{01} = 2\alpha_{10}$

Switch activity $a = \sum_i \alpha_{01,i} C_i \Big/ \sum_i C_i$

Switched capacitance $C_{sw} = a \sum_i C_i$

Dynamic power consumption $P_d = f_{clk} C_{sw} V_{pp} V_{DD}$

Short-circuit power consumption $P_{sc} = a f_{clk} t_{sc} I_{peak} V_{DD}$

Propagation time $t_p \propto V_{DD} \Big/ \left(V_{DD} - V_T\right)^r$, $1 \le r \le 2$

MOSFETs

Threshold voltage $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$

Weak inversion ($V_{GT} < 0$) $I_D = I_{D0}\left(W/L\right) e^{-\left|V_{GT}\right| / \left(n_s V_\Theta\right)} \left(1 + \lambda V_{DS}\right)$

where

$V_\Theta \approx 26$ mV @ $T = 300$ K

n_s can be calculated from $S = n_s V_\Theta \ln(10)$

Strong inversion ($V_{GT} \ge 0$) $I_D = k'\left(W/L\right) V_{min} \left(\left|V_{GT}\right| - V_{min}/2\right)\left(1 + \lambda V_{DS}\right)$

where

$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$ (corresponding to *saturation*, *resistive*, and *velocity saturation* modes)

Gate-oxide leakage $I_G = k_1 W \left(V_{ox}/t_{ox}\right)^2 e^{-k_2 t_{ox}/V_{ox}}$

Logic

Shannon's expansion theorem $\overline{f\left(x,\, y,\, z,\, \ldots,\, +,\, \cdot\right)} = f\left(\bar{x},\, \bar{y},\, \bar{z},\, \ldots,\, \cdot,\, +\right)$

Cofactors $f_{\bar{x}} = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=0}$, $f_x = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=1}$

Expansion in sum and product $f\left(x,\, y,\, z,\, \ldots\right) = \bar{x} \cdot f_{\bar{x}} + x \cdot f_x = \left(x + f_{\bar{x}}\right)\left(\bar{x} + f_x\right)$

Observability Don't Care set $\mathrm{ODC}_x = f_{\bar{x}} f_x + \overline{f_{\bar{x}}}\,\overline{f_x}$