TSTE17 System Design, CDIO
Lecture 7

- Testing
- IP
- Hints
- RF

Project hints

- Check timing of the IP blocks
  - FFT/IFFT, Viterbi block
  - Data rates, setup time, average throughput
- Selection of block and its parameters may influence the architecture
  - Setup time (before first calculation)
  - Throughput requirements
- IP blocks use serial interface with protocol
  - Collection of data put into packets

Additional information resources

- Check the websites from the manufacturer
  - Application notes shows common interfaces and applications
  - www.altera.com
- Check model examples from MATLAB
  - Demo
  - Examples
  - Web

Testing

- Four types of tests
  - Specification Test
  - Design Test
  - Implementation Test
  - Operation Test

Specification Test

- Make sure the scenarios given in the specification is correct
- Build an executable specification
- Usually requires modeling of the environment of the design

Design Test

- Make sure the functional model complies with specification
- Include filter attenuation, non-linear phase etc.

Implementation Test

- Find manufacturing errors
- Needs to be inexpensive
  - Few testpatterns

Operation Test

- Perform selftest
- Should not impact operation

Different Types

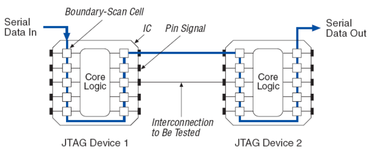
- Boundary Scan
- Built-In Self-Test
- JTAG
- Specialized tests

Boundary Scan Principle

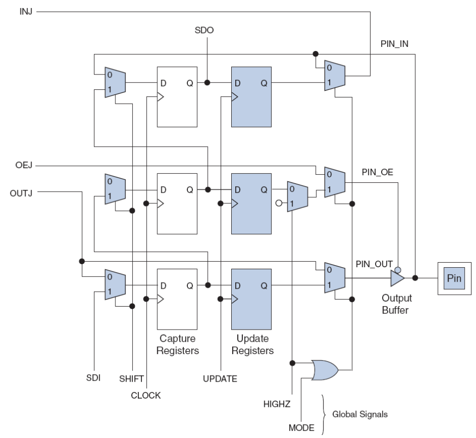
- Replacement of flip-flops with mux+flipflop
- Two modes, Test and Operational
- Tools
- Pros
  - Simple to Generate (automatized)
  - Total control of test patterns
- Cons
  - Not full speed test (timing not tested)
  - Slow (serial) test pattern updates

JTAG

- IEEE 1149 Standard
- Control each pin individually
  - Both input and output
- Special controller
  - Identify
  - Self check
- Predefined interface
  - Connect multiple chips in sequence



JTAG pin control example



Specialized Tests

- Memory blocks
  - Many different algorithms
  - Depends on technology
- Signature tests
  - CRC
  - LSFR

IP Block Problems

- IP = Intellectual property
  - Designs bought from other manufacturer
- How to test a circuit we do not have source code for?
- What boundary cases?

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FPGA debugging

- Add hardware to view internal signals
  - Multiplex if too few pins available
- Signaltap
  - Store signal in internal memory
  - Access through jtag port controller
- Test internal
  - Checksum, edge detectors, ...

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FPGA IP core models

- IP cores are described at different abstraction levels
- Different abstraction levels
  - Simulink
  - Behavoural VHDL
  - Gate Netlist VHDL
  - Gate Netlist VHDL with timing

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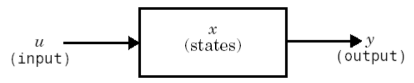
FPGA IP Core models, cont.

- Many models are handmade
  - Functionality may differ between model levels
  - IP Cores can be hardcoded macros (defines the layout)
- VHDL code import
  - Use same code for both Simulink and Behavoural VHDL
  - Automatic synthesis to gatelevel VHDL
  - Slows down simulation

Simulink internals

- Important to understand internals to debug models



$$y = f_o(t, x, u) \quad \text{output}$$
$$x_{d_{k+1}} = f_u(t, x, u) \quad \text{update}$$
$$x'_c = f_d(t, x, u) \quad \text{derivative}$$
$$\text{where} \quad x = \begin{bmatrix} x_c \\ x_{d_k} \end{bmatrix}$$

Model execution

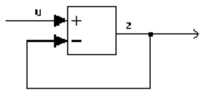
- Initializing
  - Evaluate block parameters
  - Flatten hierarchy
  - Sort blocks in update order
    - Detect algebraic loops
  - Check sample rate and vector length on interconnections
    - Forward data type and sample rate info on interconnects

Model execution simulation loop

- Simulation loop
  - Calculate next sample hit
  - Calculate outputs in major step
  - Update discrete states in major step
  - Integration
    - Calculate derivatives
    - Calculate outputs
    - Calculate derivatives
  - Locate zero crossings

Simulink simulation cont.

- Zero crossings
  - Integration of Non-discontinues signals
  - Bouncing-ball example
- Algebraic loops
  - Direct feedthrough
  - Algebraic constraint block



Simulink simulation cont.

- Discrete systems
  - Zero-order hold on outputs
  - Sampler on the inputs
  - Sample time definition
    - Scalar Ts
    - Vector [Ts, Offset] (used by discrete event blocks)

t = n * Ts + Offset

Toolboxes/block sets

- More information available by right-clicking the block in the library pane
- Simulink blockset
  - Subsystems
  - In, out
  - Enable and Trigger
  - Sources and Sinks
- Most blocks does not map to VHDL!

Possible problems

- Data type mismatch
  - Data types are sometimes propagated through the design
  - Add description of data types in the schematic
  - Force data types by adding type block

Possible problems, cont.

- Sample time
  - Sample time may be necessary to define on more than the input/output
  - Must match exact expected speed (1/3 not equal to 0.3333)
- Block execution order
  - Simulation model different
  - Use simulink debugger to find order
  - May change priority of block to force update order

Debugging help

- Use the Display menu in the simulink window
  - Shows data width, sample rate, execution order etc.
  - Use displays and scopes to visualize the signal values
  - Save values to the workspace
    - Store a log of all data into a structure
    - Show multichannel data in a readable form
  - Use the built-in Simulink Debugger

Other Simulink hints

- Use workspace I/O to partition the system
  - Run only subsystems using workspace I/O to read stimuli and store results
  - Reduces run time!
- Use vectors initially for data
  - Faster simulation
  - Less problems with synchronization
  - Frame vs Sample
- Sample time colors

DSP Systems toolbox

- Introduce concept of frames
  - Collection of time sequences
  - Designed to increase simulation speed
  - Frames can be changed into multichannel sample
- Special sources helps create frames
  - See Signal processing blockset
  - Also possible to buffer samples to create frames
  - Special casting block convert Frame <=> Sample

RF Distortion

- RF (radio frequency) subsystem have limitations
  - Peak-to-Average Power Ratio (PAPR)
  - imbalance between I and Q
  - phase noise
  - filtering of out of band signals

Components in the RF system

- IQ modulator
  - Split input data stream into two streams
  - Multiply one with sinusoidal, other with cosinusoidal waveform (baseband signal << frequency << RF)
  - Add both together to generate IF (intermediate frequency)
  - Total envelop $A=\sqrt{x_I * x_I + x_Q * x_Q}$
- Baseband Converter
  - Multiply with carrier f_c (local oscillator)

Components of the RF system cont.

- Spectral Filter
  - Limit out of band power
- Power amplificer (PA)
  - Give enough power to get reliable transmission

Amplifier Classification

- Different types of amplifiers
  - Class A
    - Continuous current flow
    - Linear region
    - Poor efficiency (25%)
  - Class B (often push-pull configuration)
    - Better efficiency
    - Poor linearity
    - Better output power

Amplifier Classification

- Class C
  - Each transistor current 0 more than 50% of the cycle
  - Better efficiency
- Class E
  - Switch on/off, use tuned output circuit
  - More efficient than Class B
  - More harmonic distortion

Amplifier imperfections

- Intermodulation (see fig 5.4)
  - near-in IM products
    - Difficult to filter out
  - other IM products possible to filter out
- Saturation
  - 1 db compression in power transfer function
- Linear region
  - noise region to saturation region

Antenna Diversity

- Use multiple antennas
  - Possible both with receiver and transmitter antennas
  - Some strategies requires knowledge about the channel
  - At 5 GHz is the channel different even with a small physical distance (0.1 – 1 m)
  - Popular name is MIMO (Multiple Input Multiple Output)
  - 802.11n allows up to 600 Mbit/s
  - LTE advanced based on MIMO (1Gbit/s)

MIMO idea

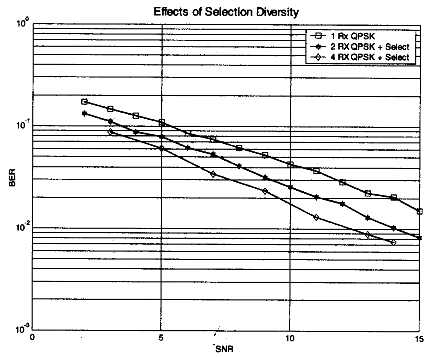
- May give increased coverage by focusing power in the correct direction
  - Beamforming Tx and/or Rx
  - May reduce effect of neighbor interferer
- May increase data rate by creating parallel beams
  - Assume independent channels by spatial diversity
  - Multipath is now required to reach high data rates!

Receive Diversity

- Use multiple receiver antennas
- Selection diversity
  - Select the one antenna with the best SNR
  - Requires no additional RF receiver chain
  - Used in some access point product for 802.11b
- Only uses information from one antenna when receiving data => Not optimal

Selection Diversity

- Rayleigh fading channel with multiple receive antenna
  - Gain of 2-3 db for two antennas
  - Gain of 3-4 db for four antennas

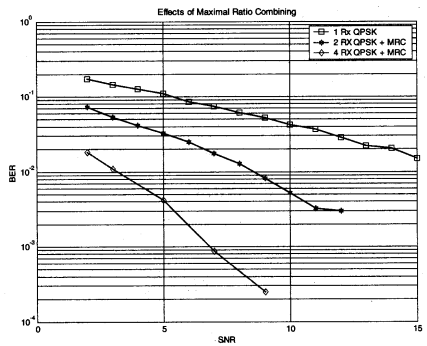


Maximal Ratio Combining

- Optimize received signal by combining all input signals
  - Compute total signal as a linear combination of all inputs
- Antennas with heavily faded signals are less important
- Requires knowledge about the channel (channel estimation)

Maximal Ration Combining

- 10 db gain with two antennas
- 15 db gain with four antennas
- Remember requirement of channel



Transmit Diversity

- Use multiple antennas to transmit information
- Multiple transmit, single receive antennas will NOT give improvement
  - Total power transmitted is still limited => Each antenna emits P/N instead of P
- Cyclic Delay Diversity
  - Send information on one at a time
  - Cycle through all antennas
  - Avoid catastrophic interference

Transmit Diversity

- Delay Diversity
  - Send the information over N antennas repeated N times non-overlapping

$$S=\begin{bmatrix} s_1 & s_2 & s_3 & s_4 & s_5 \\ 0 & s_1 & s_2 & s_3 & s_4 \\ 0 & 0 & s_1 & s_2 & s_3 \end{bmatrix}$$

  - Require knowledge about the channel
  - The receiver must solve an optimization problem, checking all possible sequences of N symbols

Layered Space-Time Codes

- Send demultiplexed data on different antennas using the same frequency and modulation
- Divide the input streams using beam forming (spatial resolution)
- Decode most important stream, considering the others as interference
- Decode the second most important stream, considering the rest as interference
- ....

Water-Filling Single Antenna

- Do not send power in channels that are faded out, or have narrow-band interference
- Two step approach
  - Power Allocation (more power if low attenuation and little noise)
  - Bit-loading (create same BER for all subcarriers)
- Requires knowledge about the channel at the transmitter
  - Possible in, e.g., ADSL

Adaptive Modulation

- Previous systems all designed for worst case channels
- If we know the channel, we can reduce power or increase data rates when the channel is good
- Change power, modulation, constellation size, and/or coding rate/scheme depending on channel
- Requires good channel estimates in the receiver that is sent with low latency to the transmitter

Antenna Diversity

- More methods are available
  - Block Space-Time Codes
  - Multidimensional Space-Time Codes
  - Sperical Space-Time Codes
  - Water-Filling in multiple antenna systems

Alternatives to OFDM

- Want to use wide band for communication
  - High datarates
- Problem caused by multipath channels
  - Fading
  - Narrow-band interference
- OFDM solved these problems by using multiple carriers

CDMA (Code Division Multiple Access)

- Spread spectrum technique
- Each transmitter is assigned a unique code sequence
  - Spreading code
  - Used to encode data to send
  - code signal bandwidth >> data signal bandwidth
- Reciever knows the code
  - Cross correlation between different users are small

CMDA Receiver

- Reciever correlates input signal with the synchronised copy of the code sequence
- Processing gain Gp = transmission bandwidth / information bandwidth

CMDA Properties

- Only the intended user signal will be despread in the correlation of the received signal.
- Can handle multipath channels
- Privacy
  - Must know the sequence to be able to detect the data
- Interference rejection
  - Cross correlation of narrowband interference will spread the interference.

CDMA Properties Cont,

- Well suited for military applications
  - Low probability of interception
    - Low power density => difficult to detect transmission
  - Antijamming capability
    - Any signal in the frequency band used for transmission will be spread in the reciever
    - Narrow-band jamming will not work

Pure CDMA

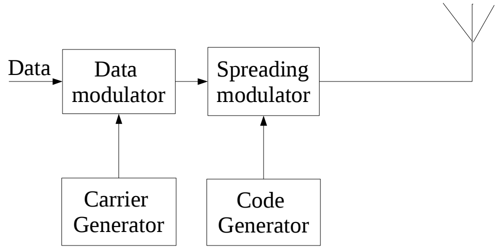
- Direct Sequence CDMA
  - Multiply information signal directly with high chip rate spreading code
- Frequency Hopping CDMA
  - Carrier frequency is rapidly changed according to a spreading code
- Time Hopping CDMA
  - Information sent in short bursts defined by the spreading code (no continous transmission)

Pure CDMA

- Two types of systems
  - averaging systems
    - Average interference over a long time
    - Direct Sequence
  - avoidance systems
    - Avoid most of the time the interference
    - Frequency Hopping
    - Time Hopping

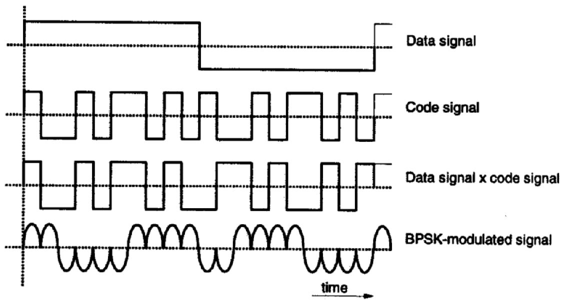
Direct Sequence CDMA

- Simple Transmitter principle
  - Code signal uses chips, consisting of -1 and 1 in a sequence (rate >> data rate)



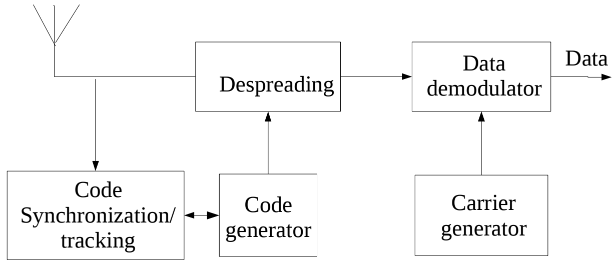
DS CMDA Transmitter

- BPSK and no data modulation example



DS CMDA Receiver

- Local code generator must be identical to transmitter and synchronized

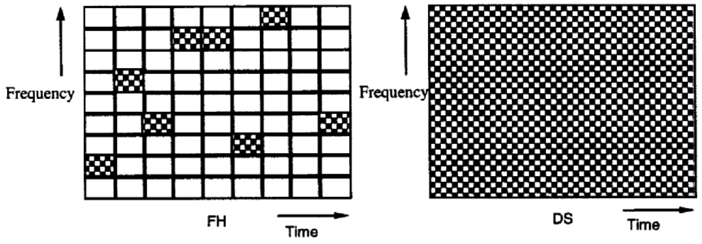


DS CDMA Properties

- Coded signal is easy to generate
- Carrier Generator easy to implement (single carrier)
- No synchronisation among users
- Difficult to aquire and maintain synchronization
- Synchronization error << chip time and nonavailable continous frequency bands => practical bandwidth limit 10-20 MHz

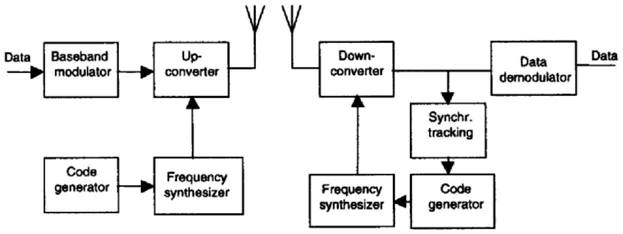
DS versus Frequency Hopping

- Both transmits the same average power in all frequency bands



Frequency Hopping

- Transmitter and Receiver structures



Frequency Hopping

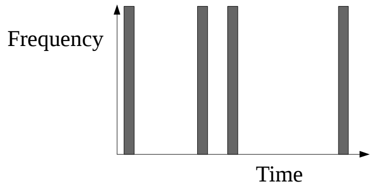
- Two types
  - Fast frequency hopping
    - Carrier frequency changes a number of times during transmission of one symbol
    - Frequency band defined by pulse shape of the hopping signal
  - Slow frequency hopping
    - Multiple symbols transmitted at the same carrier frequency
    - Frequency band used is defined by the information bandwidth

Frequency Hopping Properties

- Time synchronization easier than for DS-CDMA
- Frequency bands used in the hop sequence can be non-continous
- Better near-far performance
  - Low probability to have multiple users transmitting on the same frequency band
- Requires a sophisticated frequency synthesizer
- Coherent demodulation difficult (phase reference difficult to maintain)

Time Hopping

- Collect data into frames
- Select one timeslot according to code
- Transmit all data in this time slot



Time Hopping Properties

- Implementation is simpler than FH-CDMA
- Useful when the transmitter is average-power limited but not peak-power limited
  - Short bursts of data at high power
- Near-far problem is much less of a problem
- Takes a long time to synchronize codes
- If concurrent transmission => large data loss