# Solutions to
# Written Test
# TSEI30,
# Analog and Discrete-time Integrated Circuits

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| Date: | April 22, 2004 |
| Time: | 14 – 18 |
| Place: | U14 |
| Max. no of points: | 70;<br>50 from written test,<br>5 for project, and 15 for assignments. |
| Grades: | 30 for 3, 42 for 4, and 56 for 5. |
| Allowed material: | All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries. |
| Examiner: | Lars Wanhammar. |
| Responsible teacher: | Robert Hägglund.<br>Tel.: 0705 - 48 56 88. |
| Correct (?) solutions: | Solutions and results will be displayed in House B, entrance 25 - 27, ground floor. |

## Good Luck!

# Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

# Solutions

**1. Large-signal analysis**

The three amplifiers shown in Figure 1.1 are commonly used in for example operational amplifiers. In this exercise the analysis of these amplifier is considered. Assume that all transistor should operate in the saturation region.

a) Determine the width-over-length ratios of the two transistors in Figure 1.1a for a given output range $OR$, $V_{out,DC} = (OR_{min} + OR_{max})/2$, and current through the transistors $I$. Do not neglect the channel-length modulation nor the body effect.t

The output range is given as the voltage in which all transistors are operating in the saturation region. In order to ensure this the drain-source voltage must be at least as large as the effective voltage, i.e., the gate-source voltage minus the threshold voltage. Hence, the effective voltage for the NMOS transistor is $OR_{min}$ while it is $V_{DD} - OR_{max}$ for the PMOS transistor. Further, we can express the currents through the transistors as

$$I = I_{D1} = \alpha_1 V_{eff1}^2 (1 + \lambda V_{out,DC}) = \alpha_1 \cdot OR_{min}^2 (1 + \lambda (OR_{min} + OR_{max})/2)$$

$$\begin{aligned} I = I_{D2} &= \alpha_2 V_{eff2}^2 (1 + \lambda (V_{DD} - V_{out,DC})) \\ &= \alpha_2 (V_{DD} - OR_{max})^2 (1 + \lambda (V_{DD} - (OR_{min} + OR_{max})/2)) \end{aligned}$$

In these equations the power supply voltage, the output ranges, and the current, $I$ are given in the exercise. Hence, the width-over-length ratio can be derived by a simple rearrange in the equations. This results in

$$\frac{W_1}{L_1} = \frac{I}{OR_{min}^2 (1 + \lambda (OR_{min} + OR_{max})/2)} \cdot \frac{2}{\mu_n C_{ox}} \qquad (1.1)$$

and

$$\frac{W_2}{L_2} = \frac{I}{(V_{DD} - OR_{max})^2(1 + \lambda(V_{DD} - (OR_{min} + OR_{max})/2))} \cdot \frac{2}{\mu_p C_{ox}}$$

b) Determine the width-over-length ration of the common drain circuit shown in Figure 1.1b so that the following specification is met. The voltages $V_{in,DC}$, $V_{out,DC}$, $V_{bias}$, and the current through the transistors $I$ are given. Do not neglect the channel-length modulation nor the body effect.

The current through the transistors is expressed as

$$I = I_{D1} = \alpha_1(V_{in,DC} - V_{out,DC} - V_{T,1})^2(1 + \lambda(V_{DD} - V_{out,DC}))$$

and

$$I = I_{D2} = \alpha_2(V_{bias} - V_{T,2})^2(1 + \lambda V_{out,DC})$$

Note that the threshold voltage for transistor 1 is increased due to the body effect. This results in a threshold voltage

$$V_{T,1} = V_{T0,1} + \gamma(\sqrt{2\phi_f + V_{out,DC}} + \sqrt{2\phi_F})$$

Since the DC output voltage is given in the exercise the threshold voltage, $V_{T,1}$, can be computed directly. Further, all the voltages are fixed due to the specification as well as the current, $I$. Hence, the width-over-length ratio can be solved by rearranging the two current equations. This results in

$$\frac{W_1}{L_1} = \frac{I}{(V_{in,DC} - V_{out,DC} - V_{T,1})^2(1 + \lambda(V_{DD} - V_{out,DC}))} \cdot \frac{2}{\mu_n C_{ox}}$$

and

$$\frac{W_2}{L_1} = \frac{I}{(V_{bias} - V_{T,2})^2(1 + \lambda V_{out,DC})} \cdot \frac{2}{\mu_n C_{ox}}$$

c) Determine the input range of the common-drain amplifier shown in Figure 1.1b for the same parameters as in exercise 1b. Neglect the channel-length modulation, but not the body effect. (This exercise can be solved even though exercise 1b is not solved.)

The input range is determined as the range in which all transistors are operating in the saturation region. In this case, the input transistor limits the maximum input voltage while the biasing transistor limits the minimum possible input voltage. Starting from the lower limit of the input range. First, the minimum output voltage is determined by ensuring that the bias transistor are operating in saturation. The biasing transistor is saturated if its saturation voltage is larger than the effective voltage, i.e.,

$$V_{out,min} = V_{DS,sat,2} = V_{eff,2} = V_{bias} - V_{T,2} \tag{1.2}$$

The current through the input transistor is then

$$I_{D1} = \alpha_1(V_{in,min} - V_{out,min} - V_{T,1})^2 \tag{1.3}$$

where the threshold voltage in this case is evaluated for the source voltage

of $V_{out,\,min}$. The use of the minimum input and output voltage in Eq. (1.3) is a result of that the circuit is non inverting. From Eq. (1.3) the minimum input voltage can be solve according to

$$V_{in,\,min} = \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{out,\,min} + V_{T,\,1} = \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{bias} - V_{T,\,2} + V_{T,\,1}$$

Note, that the threshold voltage of the two transistors differ.

The maximum input voltage is determined by the input transistor. The drain-source voltage should be larger than the effective voltage, i.e.,

$$V_{DS,\,sat,\,1} = V_{DD} - V_{out,\,max} = V_{eff,\,1} = V_{in,\,max} - V_{out,\,max} - V_{T,\,1}$$

From this equation can solve for $V_{in,\,max} = V_{DD} + V_{T,\,1}$. Notice that the threshold voltage in this case is computed for the source voltage of $V_{out,\,max}$.

d) Determine the width-over-length ratio for the transistors in the amplifier in Figure 1.1c to meet the following specification. The current through the transistors, $I$, and the voltages $V_{in,\,DC}$, $V_{out,\,DC}$, $V_{bias1}$, and $V_{bias2}$ are given. Do not neglect the channel-length modulation nor the body effect.

First, compute the current through the transistors

$$I = I_{D1} = \alpha_1(V_{bias1} - V_{in,\,DC} - V_{T,\,1})^2(1 + \lambda(V_{out,\,DC} - V_{in,\,DC}))$$

$$I = I_{D2} = \alpha_2(V_{DD} - V_{bias2} - V_{T,\,2})^2(1 + \lambda(V_{DD} - V_{out,\,DC}))$$

Solve for the width-over-length ratio in both equations results in

$$\frac{W_1}{L_1} = \frac{I}{(V_{bias1} - V_{in,\,DC} - V_{T,\,1})^2(1 + \lambda(V_{out,\,DC} - V_{in,\,DC}))}\frac{2}{\mu_n C_{ox}}$$

and

$$\frac{W_2}{L_2} = \frac{I}{(V_{DD} - V_{bias2} - V_{T,\,2})^2(1 + \lambda(V_{DD} - V_{out,\,DC}))}\frac{2}{\mu_p C_{ox}}$$

The threshold voltage of transistor M1 is computed by the formula

$$V_{T,\,1} = V_{T0,\,1} + \gamma(\sqrt{2\phi_f + V_{in,\,DC}} + \sqrt{2\phi_F}) \qquad (1.4)$$

e) Determine the output range of the amplifier shown in Figure 1.1c for the same parameters as in exercise 1d (This exercise can be solved even though exercise 1d is not solved.)

The maximum output voltage is determined by the saturation voltage of the PMOS transistor, i.e.,

$$V_{out,\,max} = V_{DD} - V_{SD,\,sat,\,2} = V_{DD} - V_{eff,\,2} = V_{DD} - V_{bias2} - V_{T,\,2}$$

The minimum output voltage is determined as the voltage for which the transistor M1 is saturated. Hence, in this case the $V_{eff,\,1} = V_{DS,\,sat,\,1}$ which results in the following equation

$$V_{bias1} - V_{in,\,min} - V_{T,\,1} = V_{out,\,min} - V_{in,\,min} \tag{1.5}$$

Solving for the minimum output voltage results in

$$V_{out,\,min} = V_{bias1} - V_{T,\,1} \tag{1.6}$$

where $V_{T,\,1}$ is evaluated according to $V_{T,\,1} = V_{T0,\,1}$ since the minimum input voltage is assumed to be ground.

## 2. Small-signal analysis

The transistors in the circuit shown in Figure 2.1 are biased in the saturation region. Neglect the influence of all internal parasitics in the transistors.

a) Compute the transfer function of the circuit shown in Figure 2.1a, $H(s) = V_{out}(s)/V_{in}(s)$. Do not neglect the bulk effect.

The small-signal model of the amplifier is shown in Figure 2.1

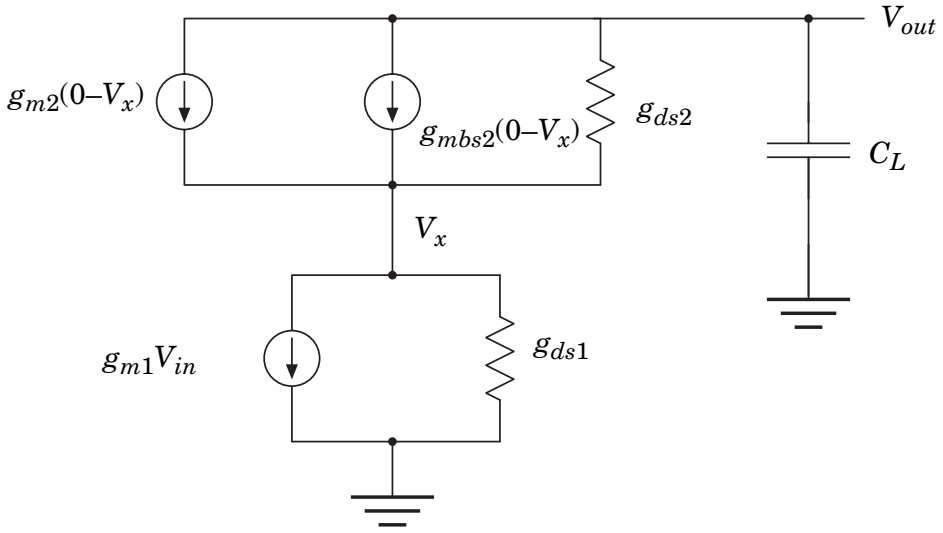


***Figure 2.1*** The small-signal model of the common-source amplifier with cascodes.

The transfer function from the input to the output is computed by for example applying nodal analysis. This gives the following set of equations

$$g_{m1}V_{in} + V_x g_{ds1} + (g_{m2} + g_{mbs2})V_x + (V_x - V_{out})g_{ds2} = 0 \tag{2.1}$$

$$(g_{m2} + g_{mbs2})V_x + (V_x - V_{out})g_{ds2} - V_{out}sC_L = 0 \tag{2.2}$$

Solving the voltage $V_x$ as a function of the output voltage from Eq. (2.2) results in

$$V_x = \frac{g_{ds2} + sC_L}{g_{m2} + g_{mbs2} + g_{ds2}} V_{out} \tag{2.3}$$

Inserting this into Eq. (2.1) results in

$$g_{m1}V_{in} = V_{out}\left(g_{ds2} - \frac{(g_{m2}+g_{mbs2}+g_{ds2}+g_{ds1})(g_{ds2}+sC_L)}{g_{m2}+g_{mbs2}+g_{ds2}}\right)$$

Performing some simplifications

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= -\frac{g_{m1}}{\dfrac{g_{ds2}g_{ds1}}{g_{m2}+g_{mbs2}+g_{ds2}} + sC_L\left(1+\dfrac{g_{ds1}}{g_{m2}+g_{mbs2}+g_{ds2}}\right)} \\ &= -\frac{g_{m1}}{\dfrac{g_{ds2}g_{ds1}}{g_{m2}+g_{mbs2}+g_{ds2}}}\frac{1}{1+\dfrac{s}{\dfrac{\dfrac{g_{ds2}g_{ds1}}{g_{m2}+g_{mbs2}+g_{ds2}}+g_{ds2}}{C_L}}}\end{aligned} \qquad (2.4)$$

b) Express the DC gain and unity-gain frequency of the circuit shown in Figure 2.1a in terms of relevant design parameters ($\alpha$, $I_{bias}$, ...).

The small-signal parameters can be expressed as a function of the $\alpha$-factor, the drain current, and the channel-length modulation factor, $\lambda$. However, this can only be performed for a simplified model of the circuit in order to arrive at a useful expression. Hence, approximate expressions for the DC gain and the unity-gain frequency are of interest.

$$A_0 = -\frac{g_{m1}}{\dfrac{g_{ds2}g_{ds1}}{g_{m2}+g_{mbs2}+g_{ds2}}} \approx -\frac{g_{m1}}{\dfrac{g_{ds1}g_{ds2}}{g_{m2}}} \propto \frac{\sqrt{\alpha_1 I_{bias}}\sqrt{\alpha_2 I_{bias}}}{\frac{1}{L_1}\frac{1}{L_2}I_{bias}^2} \propto \frac{\sqrt{W_1L_1W_2L_2}}{I_{bias}}$$

The unity-gain frequency is typically given as the DC gain time the first pole if the DC gain is large which is the case when the transistors are operating in the saturation region.

$$\omega_u \approx |A_0|p_1 \approx \frac{g_{m1}}{\dfrac{g_{ds1}g_{ds2}}{g_{m2}}}\frac{\dfrac{g_{ds2}g_{ds1}}{g_{m2}}}{C_L} = \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\dfrac{W_1}{L_1}I_{bias}}}{C_L}$$

c) Derive the transfer function of the circuit shown in Figure 2.1b, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. Do not neglect the bulk effect. The gain $A_I$ is a negative, real constant.

The small-signal model of the common-source amplifier with gain boosting is shown in Figure 2.2. The transfer function can be compute by for example nodal analysis. The following equations is then obtained

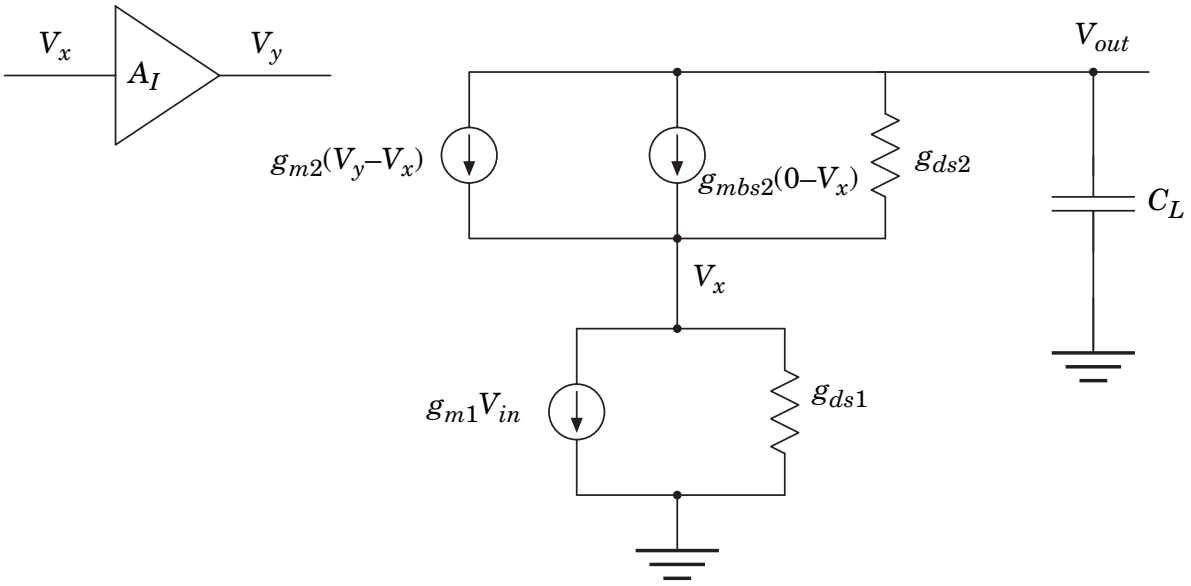


***Figure 2.2*** The small-signal model of the common-source amplifier with gain-boosting.

$$g_{m1}V_{in} + V_x g_{ds1} + g_{m2}(V_x - V_y) + (V_x - V_{out})g_{ds2} + g_{mbs2}V_x = 0$$

$$(g_{m2} + g_{mbs2})(V_x - V_y) + (V_x - V_{out})g_{ds2} - V_{out}sC_L = 0$$

$$V_y = A_I V_x$$

This system of equations can be solved in using several approaches. In this case the $V_y$ voltage is eliminated from the two topmost equations. The second equation is solved for $V_x$. This results in

$$V_x = \frac{g_{ds2} + sC_L}{g_{m2}(1 - A_I) + g_{mbs2} + g_{ds2}} V_{out} \tag{2.5}$$

Eliminating $V_x$ from the first equation results in

$$g_{m1}V_{in} = V_{out}\left(g_{ds2} - \frac{(g_{ds1} + g_{ds2} + (g_{m2} + g_{mbs2})(1 - A_I))(g_{ds2} + sC_L)}{g_{m2}(1 - A_I) + g_{mbs2} + g_{ds2}}\right)$$

This can be simplified to

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\dfrac{g_{ds2}g_{ds1}}{g_{m2}(1 - A_I) + g_{mbs2} + g_{ds2}} + sC_L\left(1 + \dfrac{g_{ds1}}{g_{m2}(1 - A_I) + g_{mbs2} + g_{ds2}}\right)}$$

d) Express the DC gain and unity-gain frequency of the circuit shown in Figure 2.1b in terms of relevant design parameters ($\alpha$, $I_{bias}$, ...).

The DC gain can be identified from the transfer function by setting the *s* parameter to zero. This results in a DC gain of

$$A_0 = -\frac{g_{m1}}{\dfrac{g_{ds2}g_{ds1}}{g_{m2}(1-A_I)+g_{mbs2}+g_{ds2}}} \approx -\frac{g_{m1}}{\dfrac{g_{ds1}g_{ds2}}{g_{m2}A}} \propto \frac{\sqrt{W_1L_1W_2L_2}}{I_{bias}}\frac{1}{-A_I}$$

The unity-gain frequency is still given by the expression $\omega_u \approx |A_0|p_1$ which results in

$$\omega_u \approx \frac{g_{m1}}{\dfrac{g_{ds1}g_{ds2}}{g_{m2}(-A_I)}} \frac{\dfrac{g_{ds1}g_{ds2}}{g_{m2}(1-A_I)+g_{mbs2}+g_{ds2}} + g_{ds2}}{C_L} \approx \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\dfrac{W_1}{L_1}I_{bias}}}{C_L}$$

Hence, the unity-gain frequency is approximately equal for the two circuits while the DC gain has increased by a factor $A_I$ due to the additional amplifier used as a gain-boosting device.

## 3. Operational amplifiers

The trend is to decrease the minimum feature sizes in modern CMOS process. This causes the low-frequency gain of a single transistor to decrease. If high DC gain is required in a modern process a multi-stage amplifier may be a good choice. In this exercise, a small-signal equivalent of the differential response of a three stage amplifier shown in Figure 3.1a is considered. The common-mode gain is zero. Throughout this exercise, assume that $C_L \gg C_1 = C_2 = C$, $R_1 = R_2 = R_L = R$.

a) Derive the transfer function from the input to the output of the circuit shown in Figure 3.1a, i.e., $H(s) = V_{out}(s)/V_{in,\,diff}(s)$.

Since there are not direct connections (compensations) between the individual gain stages in this circuit the transfer function can be divided into a product of partial transfer functions, i.e.,

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_2}\frac{V_2}{V_1}\frac{V_1}{V_{in}} = \frac{A_3}{1+sR_LC_L}\cdot\frac{A_2}{1+sR_2C_2}\cdot\frac{A_1}{1+sR_1C_1} \qquad (3.1)$$

b) Compute an approximative expression for the unity-gain frequency given that the higher-order poles are located at much higher frequency than the unity-gain frequency. Motivate your solution.

Due to the simplification mentioned above, the transfer function can be reformulated to

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{A_0}{\left(1+\dfrac{s}{p_1}\right)\left(1+\dfrac{s}{p_2}\right)^2} \qquad (3.2)$$

where $p_1 = 1/(R_LC_L)$, $p_2 = 1/(RC)$, and $A_0 = A_1A_2A_3$.

The unity-gain frequency of the amplifier is computed as $|H(j\omega_u)| \equiv 1$

$$\frac{A_0^2}{\left(1+\frac{\omega_u^2}{p_1^2}\right)\left(1+\frac{\omega_u^2}{p_2^2}\right)^2} = 1 \qquad \Rightarrow \qquad A_0^2 = \left(1+\frac{\omega_u^2}{p_1^2}\right)\left(1+\frac{\omega_u^2}{p_2^2}\right)^2$$

This equation may be hard to solve exactly. However, an approximate solution is obtained by assuming that $|p_2| \gg \omega_u$. This assumption causes the term

$$\left(1+\frac{\omega_u^2}{p_2^2}\right)^2 \approx 1 \tag{3.3}$$

Hence, the approximated equation is now

$$A_0^2 \approx 1+\frac{\omega_u^2}{p_1^2} \tag{3.4}$$

which results in the following approximate expression for the unity-gain frequency

$$\omega_u \approx p_1\sqrt{A_0^2-1} \approx |A_0|p_1 \tag{3.5}$$

This expression holds if higher-order poles do not contribute so much to the decrease in the magnitude response and that the DC gain is much larger than unity (which is the case here).

c) The amplifier is connected in a close-loop configuration as shown in Figure 3.1b. For such a circuit, the transfer function can be given in the form

$$H(s) = \frac{A(s)}{1+\beta A(s)} \tag{3.6}$$

where $\beta$ is the feedback factor and $A(s)$ is the gain of the amplifier. Determine the feedback factor for the circuit shown in Figure 3.1b..

This exercise is solved by computing the transfer function from the input of the amplifier in the feedback configuration to its output. In this case the characteristics of the amplifier is

$$(V_{in,\,\mathrm{amp}+} - V_{in,\,\mathrm{amp}-})A = V_{out,\,\mathrm{opamp}}$$

Inserting this into the buffer connected circuit the result is

$$(V_{in}-V_{out})A = V_{out} \qquad \Rightarrow \qquad \frac{V_{out}}{V_{in}} = \frac{A}{1+A}$$

Hence, the feedback factor $\beta$ is unity.

d) For the circuit in Figure 3.1b compute an analytic expression for the factor $K$, which relates the second pole $p_2$ and the unity-gain frequency $\omega_u$, in the expression $p_2 = K \cdot \omega_u$ in order to obtain a specific phase margin, i.e., compute $K = f(\phi_m)$. Assume that at the unity-gain frequency the first pole has caused a –90 degree phase shift.

The phase margin of the circuit for $\beta = 1$ is computed as follows

$$\phi_m = -\text{atan}\frac{\omega_u}{p_1} - 2\,\text{atan}\frac{\omega_u}{p_2} + 180 = -\text{atan}\frac{\omega_u}{p_1} - 2\,\text{atan}\frac{1}{K} + 180$$

From the exercise the first term in the equation for the phase margin is –90 degrees. Hence, the phase margin is

$$\phi_m = 90 - 2\,\text{atan}\frac{1}{K} \tag{3.7}$$

Solving for the K factor results in

$$K = \frac{1}{\tan\left(\frac{90 - \phi_m}{2}\right)} \tag{3.8}$$

e) Compute the value of the $K$ factor to obtain a phase margin of 45 and 75 degrees, respectively.

Using Eq. (3.8) for the phase margins of 45 and 75 degrees respectively results in that the higher-order poles must be located at 2.4 and 7.6 time the unity-gain frequency.

f) Is the approximation in 3b good for the two cases in exercise 3e? Motivate your answer carefully.

Here it is not so easy to give a yes or no answer since this will depend on the application. However, in the computation of the approximate expression for the unity-gain frequency we obtained the following expression

$$A_0^2 = \left(1 + \frac{\omega_u^2}{p_1^2}\right)\left(1 + \frac{\omega_u^2}{p_2^2}\right)^2 \tag{3.9}$$

which should be solved with respect to the unity-gain frequency. In the approximate expression the second term was set to zero since $|p_2| \gg \omega_u$. For a phase margin of 45 degrees $|p_2| \approx 2.4\omega_u$ which results in value of the second term in Eq. (3.9) to be equal to about 1.37. Hence, the unity-gain frequency is a little bit smaller than for the estimation.

For the case of 75 degree phase margin the second term is about 1.035 which typically is small enough for many of the hand computation tasks.

## 4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time $t$, $t + 2\tau$, $t + 4\tau$, is shown in Figure 4.1.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the operational amplifier is ideal.

Starting by assigning positive charge at the left plate of capacitor $C_1$ and to the top of capacitor $C_2$, $C_3$, and $C_4$. Further, the voltage at the positive input node of the operational amplifier is called $V_x$. The next step is to express the charge at the capacitors.

At time $t$

$q_1(t) = C_1V_1(t)$, $q_2(t) = 0$, $q_3(t) = C_3(0 - V_2(t))$, $q_4(t) = C_4V_x(t)$

time $t + \tau$

$q_1(t+\tau) = C_1(V_x(t+\tau) - V_{out}(t+\tau))$, $q_2(t+\tau) = C_2 V_x(t+\tau)$,
$q_3(t+\tau) = C_3(V_x(t+\tau) - V_{out}(t+\tau))$, $q_4(t+\tau) = C_4 V_{out}(t+\tau)$

and at time $t + 2\tau$

$q_1(t+2\tau) = C_1 V_1(t+2\tau)$, $q_2(t+2\tau) = 0$, $q_3(t+2\tau) = C_3(0 - V_2(t+2\tau))$,
$q_4(t+2\tau) = C_4 V_x(t+2\tau)$

The charge conservation equations are

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = q_1(t) + q_2(t) + q_3(t) \tag{4.1}$$

$$q_4(t+2\tau) = q_4(t+\tau) \tag{4.2}$$

The Eq. (4.2) results in

$$C_4 V_x(t+2\tau) = C_4 V_{out}(t+\tau) \tag{4.3}$$

which states that the output voltage at clock phase 2 is equal to the $V_x$ voltage at the next clock phase.

Furthermore, Eq. (4.1) results in

$$C_1(V_x(t+\tau) - V_{out}(t+\tau)) + C_2 V_x(t+\tau) + C_3(V_x(t+\tau) - V_{out}(t+\tau)) = \\ = C_1 V_1(t) + C_3(0 - V_2(t))$$

This can be simplified to

$$C_1 V_1(t) - C_3 V_2(t) = (C_1 + C_3)(V_x(t+\tau) - V_x(t+2\tau)) + C_2 V_x(t+\tau) \tag{4.4}$$

Since the amplifier is ideal, the voltage difference between the positive and negative input terminals is zero, this results in that
$V_{out}(t+\tau) = V_x(t+\tau) = V_x(t+2\tau)$. The resulting expression is then

$$C_1 V_1(t) - C_3 V_2(t) = C_2 V_{out}(t+2\tau) \tag{4.5}$$

Performing a Z-transformation on this equation gives the results

$$V_{out}(z) = \left(\frac{C_1}{C_2} V_1(z) - \frac{C_3}{C_2} V_2(z)\right) z^{-1} \tag{4.6}$$

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The parasitics of interest are shown in Figure 4.1.

$C_{pa}$, $C_{pf}$ do not alter the transfer function since they are always connected to the ideal input source.

$C_{pb}$ changes the transfer function since in clock phase 1 it is charged and in clock phase 2 it is discharged to a sensitive node. It takes part of a charge redistribution.

$C_{pc}$ Connected between output node of OPamp to ground. No changes in the transfer function.

$C_{pd}$ Connected between ground and virtual ground which results in no change in the transfer function

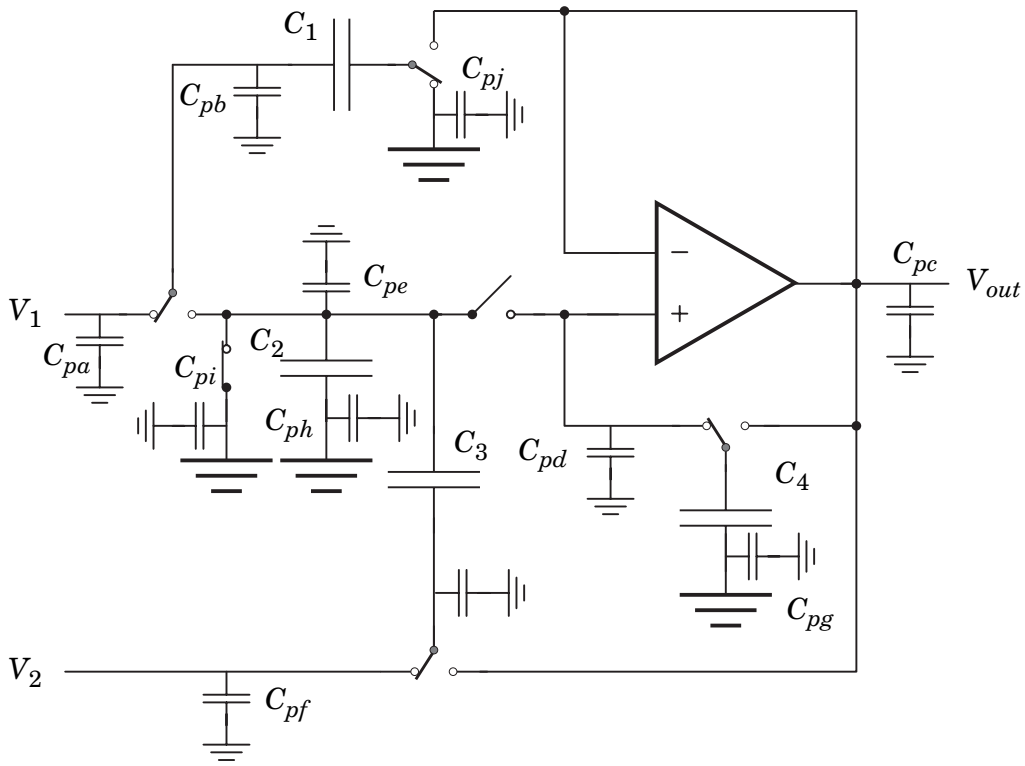


***Figure 4.1*** The SC circuit with capacitive parasitics due to the capacitor and the switches.

$C_{pe}$ Connected between ground and ground or virtual ground and ground. No effect on the transfer function.

$C_{pg}$, $C_{ph}$, $C_{pi}$, $C_{pj}$ Connected between ground and ground not changing the transfer function.

Hence, the circuit is sensitive to capacitive parasitics, when the transfer function is of concern.

c) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA has finite gain, $A$.

The solution will follow that in a) until Eq. (4.4), here restated for convenience

$$C_1V_1(t) - C_3V_2(t) = (C_1 + C_3)(V_x(t+\tau) - V_x(t+2\tau)) + C_2V_x(t+\tau) \tag{4.7}$$

For an opamp with finite gain the difference between the positive and the negative input terminals is given by

$$(V_{inp} - V_{inn})A = V_{out} \qquad \Rightarrow \qquad (V_x - V_{out})A = V_{out}$$

for both clock phases. Solving for the $V_x$ voltage as a function of the output voltage results in

$$V_x(t) = V_{out}(t)\left(\frac{1}{A} + 1\right) \tag{4.8}$$

and

$$V_x(t+\tau) = V_{out}(t+\tau)\left(\frac{1}{A}+1\right) \tag{4.9}$$

Hence, the Eq. (4.7) can be reformulated as

$$C_1V_1(t) - C_3V_2(t) = (C_1+C_3)\left(V_x(t+\tau) - V_{out}(t+2\tau)\left(\frac{1}{A}+1\right)\right) + C_2V_{out}(t+\tau) \tag{4.10}$$

Further, the relation that $V_{out}(t+\tau) = V_x(t+2\tau)$ is used to combine Eq. (4.8) and Eq. (4.9) with the result

$$V_x(t+\tau) = V_{out}(t+2\tau)\left(\frac{1}{A}+1\right)^2$$

Inserting this equation into Eq. (4.10) gives

$$C_1V_1(t) - C_3V_2(t) = \left((C_1+C_3)\left(1+\frac{1}{A}\right)\left(-\frac{1}{A}\right) + C_2\left(\frac{1}{A}+1\right)^2\right)V_{out}(t+2\tau)$$

Performing a Z-transformation and a rearranging of the equation results in the following relation

$$V_{out}(z) = \frac{C_1V_1(z) - C_3V_2(z)}{(C_1+C_3)\left(1+\frac{1}{A}\right)\left(-\frac{1}{A}\right) + C_2\left(\frac{1}{A}+1\right)^2}z^{-1} \tag{4.11}$$

Hence, the finite gain of the amplifier results in a decrease in the gain of the amplification.

## 5. A mixture of questions

a) Design the circuit shown in Figure 5.1 so that $V_{in,DC} = V_{out,DC} = V_{DD}/2$. Draw the small-signal model for this circuit and compute its DC gain.

The current through the transistors are

$$I_{D1} = \alpha_1(V_{in} - V_{T,1})^2(1+\lambda_1V_{out}) \tag{5.1}$$

$$I_{D2} = \alpha_2(V_{DD} - V_{in} - V_{T,2})^2(1+\lambda_2(V_{DD} - V_{out})) \tag{5.2}$$

Inserting the equation $V_{in,DC} = V_{out,DC} = V_{DD}/2$ results in

$$I_{D1} = \alpha_1\left(\frac{V_{DD}}{2} - V_{T,1}\right)^2\left(1+\lambda_1\frac{V_{DD}}{2}\right) \tag{5.3}$$

$$I_{D2} = \alpha_2\left(\frac{V_{DD}}{2} - V_{T,2}\right)^2\left(1+\lambda_2\frac{V_{DD}}{2}\right) \tag{5.4}$$

The inverter should be size so that

$$\frac{\alpha_1}{\alpha_2} = \frac{\left(\frac{V_{DD}}{2} - V_{T,2}\right)^2\left(1 + \lambda_2\frac{V_{DD}}{2}\right)}{\left(\frac{V_{DD}}{2} - V_{T,1}\right)^2\left(1 + \lambda_1\frac{V_{DD}}{2}\right)} \tag{5.5}$$

The small-signal model of the circuit is shown in Figure 5.1. The DC gain of the circuit is computed by the use of nodal analysis

$$V_{in}(g_{m1} + g_{m2}) + V_{out}(g_{ds1} + g_{ds2}) = 0 \tag{5.6}$$

and the DC gain is

$$A_0 = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \tag{5.7}$$

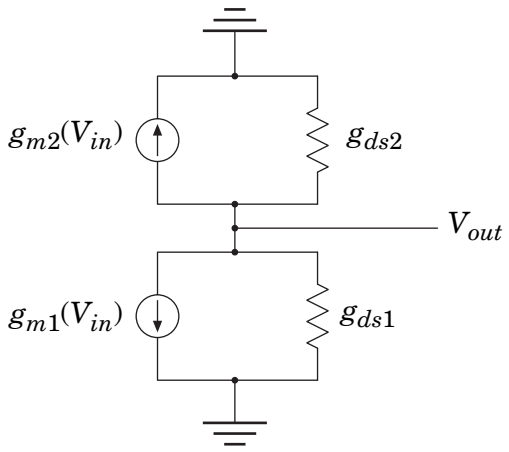


***Figure 5.1*** A small-signal model for a CMOS inverter

b) State one reason why it is uncommon to use the minimum channel length of a transistor in an analog circuit.

The minimum channel length is not commonly used since the $\beta$ matching is poor for this choice of channel length. Instead, larger channel lengths are commonly used.

c) State benefits and drawbacks of using a fully differential compare with a single-ended circuit structure in an integrated analog circuit.

Benefits of using fully differential circuits are decreased noise at the outputs, increased CMRR and PSRR. Suppression of even-order distortion terms. The drawbacks are increased power consumption and the need for a common-mode output stabilization circuit.

d) Compute the input impedance of the circuit shown in Figure 5.2, i.e., $Z_{in}(s) = V_{in}(s)/I_{in}(s)$. Assume that the operational amplifier is ideal. Further, select appropriate components (resistor or capacitors, but not inductors) for the impedances, $Z_i$, so that the circuit realizes an inductor.

The input impedance of the circuit is computed by computing the current delivered by the input voltage source. Ideal opamps results in that the input

voltage difference between the positive and negative terminal is zero. Hence, the voltage in nodes $V_b$ and $V_L$ in Figure 5.2 is the same as the input voltage, $V_{in}$.

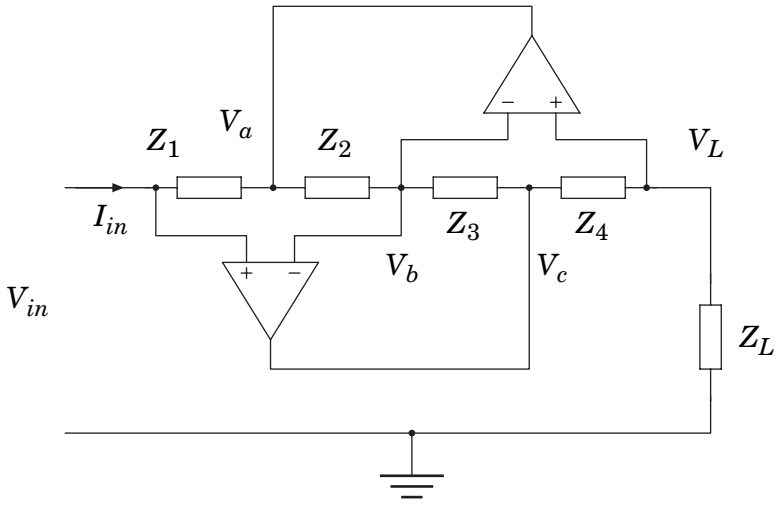


***Figure 5.2*** A circuit that can be used to realize an inductor.

The voltage drop over the impedance $Z_1$ should equal minus the drop over $Z_2$, i.e., $Z_1 I_1 = -Z_2 I_2$. Further, $I_2 = I_3$, $Z_3 I_3 = -Z_4 I_4$ and

$$I_4 = I_L = \frac{V_{in}}{Z_L}$$

Hence,

$$I_1 = I_{in} = -\frac{Z_2}{Z_1} I_2 = -\frac{Z_2}{Z_1} \cdot -\frac{Z_4}{Z_3} \cdot \frac{V_{in}}{Z_L}$$

which results in the input impedance equal to

$$\frac{V_{in}}{I_{in}} = \frac{Z_1 Z_3}{Z_2 Z_4} Z_L$$

In order to realize an inductor the impedances $Z_1$, $Z_2$, $Z_3$, and $Z_L$ can be realized by resistors while $Z_4$ is a capacitor.