Solutions to written exam
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	Mars 12, 2003
Time:	14 – 18
Place:	U1 and T2
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

a) Sketch the output voltage as a function of the input voltage ($V_{out} = f(V_{in})$) for the input voltage between ground and the power supply voltage.

b) Determine the operation region of the transistor in the different parts of the figure sketched in a).

The transistor is cut-off for high input voltages. The bulk is connected to the power supply voltage. Hence, the threshold voltage is not varied with the operating point. When the transistor is operating in the cut-off region($V_{in} > V_{DD} - V_T$) the current through the device is small (approximately zero) and the output voltage is zero (since the voltage over the resistor is the resistance times the current). Decreasing the input voltage will result in a transistor operating in the saturation region since the drain-source voltage (the power supply voltage minus the output is larger than the effective voltage). The current is increasing approximately quadratically due to the transistor model. For low input voltage the drain-source voltage is smaller than the effective voltage and the transistor operates in the linear region. The output voltage increases linearly. (This can be seen as two resistors in series where the top resistor is varible.

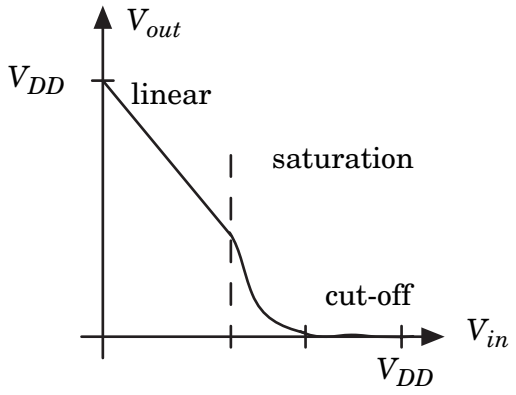

Figure 1.1 The output voltage as a function of the input voltage.

c) Determine the input and output voltage when the transistor switches from operating in the saturation region to operate in the linear region. Neglect the influence of the channel-length modulation.

The voltage when the transistor is switching from the saturation region to the linear region is when the drain-source voltage equals the effective voltage. Hence,

$$V_{SD} = V_{SG} - V_T = V_{eff} \tag{1.1}$$

The current is the saturation region is given by $I_D = \alpha(V_{DD} - V_{in} - V_T)^2$ when the channel-length modulation is neglected. Further, the source-drain voltage is given by $V_{DD} - V_{out}$ and the output voltage is determined by $V_{out} = RI_D$. Inserting Eq. (1.1) into the current equation yields

$$\frac{V_{out}}{R} = \alpha(V_{DD} - V_{out})^2 \tag{1.2}$$

which can be simplified to

$$V_{out}^2 - V_{out}\left(\frac{1}{\alpha R} + 2V_{DD}\right) + V_{DD}^2 = 0 \tag{1.3}$$

Hence, the output voltage is

$$V_{out} = \frac{1}{2\alpha R} + V_{DD} \pm \sqrt{\left(\frac{1}{2\alpha R} + V_{DD}\right)^2 - V_{DD}^2} \tag{1.4}$$

which can be simplified to

$$V_{out} = \frac{1}{2\alpha R} + V_{DD} \pm \sqrt{\frac{1}{4\alpha^2 R^2} + \frac{V_{DD}}{\alpha R}} \tag{1.5}$$

Where the plus solution is outside the interval.

The input voltage is $V_{DD} - V_{in} = V_{DD} - V_{out} - V_T$ according to Eq. (1.1). Hence, the input voltage is

$$V_{in} = V_{out} + V_T = \frac{1}{2\alpha R} + V_{DD} + V_T \pm \sqrt{\frac{1}{4\alpha^2 R^2} + \frac{V_{DD}}{\alpha R}} \tag{1.6}$$

2. Small-signal analysis

a) The circuit can be decomposed into two different parts, i.e., the PMOS transistor and the resistor R_1 and the NMOS transistor and the resistor R_2. The PMOS transistor and R_1 can in a small-signal sense be reduced to a resistor. Derive an expression for the equivalent resistor, R_{eq}.

The small-signal model of the PMOS and resistor part is shown in Figure 2.1. The impedance of the amplifier is computed by adding a current source at the output and computing the current through the device. The current is computed using the nodal analysis in node V_y and V_{out}. The nodal analysis gives the following equations

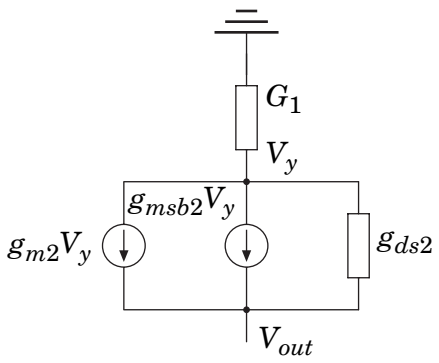

Figure 2.1 The small-signal model of the PMOS part of the amplifier.

$$V_y G_1 + g_{m2}V_y + g_{mbs2}V_y + (V_y - V_{out})g_{ds2} = 0 \tag{2.1}$$

$$g_{m2}V_y + g_{mbs2}V_y + (V_y - V_{out})g_{ds2} + I_{out} = 0 \tag{2.2}$$

The voltage in node V_y can be computed as a function of the output voltage from the results in Eq. (2.1). This yields

$$V_y = \frac{g_{ds2}V_{out}}{g_{m2} + g_{mbs2} + g_{ds2} + G_1} \tag{2.3}$$

Inserting this into Eq. (2.2) yields

$$I_{out} = V_{out}\left(g_{ds2} - (g_{m2} + g_{mbs2} + g_{ds2})\frac{g_{ds2}}{g_{m2} + g_{mbs2} + g_{ds2} + G_1}\right)$$

which is simplified to

$$I_{out} = V_{out}\left(g_{ds2}\frac{G_1}{g_{m2} + g_{mbs2} + g_{ds2} + G_1}\right) \tag{2.4}$$

and the resistance is then

$$R_{eq} = \frac{V_{out}}{I_{out}} = \frac{g_{m2} + g_{mbs2} + g_{ds2} + G_1}{G_1 g_{ds2}} \approx$$

$$\approx \frac{g_{m2}}{G_1 g_{ds1}} + \frac{1}{g_{ds1}} \tag{2.5}$$

b) Derive the small-signal gain and the first pole of the amplifier shown in the figure, where the PMOS transistor and R_1 is substituted with an equivalent resistance, R_{eq}. The expressions should be functions containing R_{eq}.

The small-signal model of the amplifier is shown in Figure 2.2.

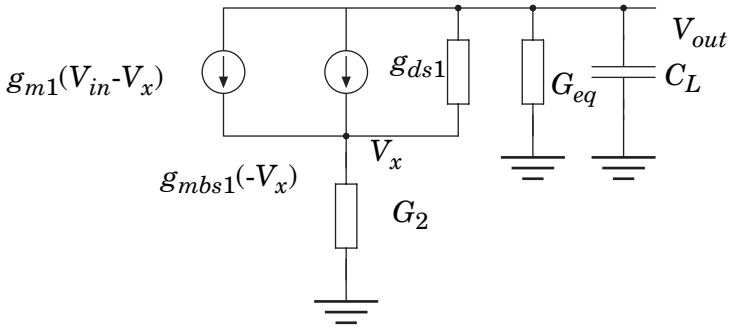

Figure 2.2 The small-signal model of the amplifier.

The transfer function is found by utilizing nodal analysis in nodes V_x and V_{out}.

$$g_{m1}(V_{in}-V_x)-V_x g_{mbs1}+(V_{out}-V_x)g_{ds1}-V_x G_2 = 0$$

$$g_{m1}(V_{in}-V_x)-V_x g_{mbs1}+(V_{out}-V_x)g_{ds1}+V_{out}(G_{eq}+sC_L)$$

Solving this system of equations yields

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\dfrac{(g_{m1}+g_{mbs1}+g_{ds1}+G_2)G_{eq}+G_2 g_{ds1}}{G_2}+\dfrac{sC_L(g_{m1}+g_{mbs1}+g_{ds1}+G_2)}{G_2}}$$

Hence, the DC gain is given by

$$A_0 = -\frac{g_{m1}}{\dfrac{(g_{m1}+g_{mbs1}+g_{ds1}+G_2)G_{eq}+G_2 g_{ds1}}{G_2}} \approx -\frac{g_{m1}}{\dfrac{(g_{m1}+G_2)G_{eq}+G_2 g_{ds1}}{G_2}}$$

and the first pole by

$$p_1 = \frac{(g_{m1}+g_{mbs1}+g_{ds1}+G_2)G_{eq}+G_2 g_{ds1}}{(g_{m1}+g_{mbs1}+g_{ds1}+G_2)C_L} = \frac{G_{eq}}{C_L}+\frac{G_2 g_{ds1}}{(g_{m1}+g_{mbs1}+g_{ds1}+G_2)C_L}$$

3. Macro blocks

a) Derive the transfer function from the input to the output of the circuit, $H(s) = V_{out}(s)/V_{in}(s)$.

The gain of the amplifier is finite, hence, the output of the amplifier is

$$V_{out} = A(s)(V_{inp,\,amplifier}-V_{inn,\,amplifier}) \qquad (3.1)$$

which means that the voltage at the negative input terminal is

$$V_{inn,\,amplifier} = -\frac{V_{out}}{A(s)}. \qquad (3.2)$$

Using nodal analysis yields

$$\frac{V_{in} - V_{inn,\,amplifier}}{R_1} = \frac{V_{inn,\,amplifier} - V_{out}}{R_2} + (V_{inn,\,amplifier} - V_{out})sC_1$$

Combining this equation with Eq. (3.2) yields

$$R_2 V_{in} = -\frac{V_{out}}{A(s)}(R_1 + R_2 + sC_1R_1R_2) - V_{out}(R_1 + sC_1R_1R_2)$$

Hence, the transfer function is

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{\frac{R_1 + R_2 + sC_1R_1R_2}{A(s)} + R_1 + sC_1R_1R_2} = \tag{3.3}$$

which can be simplified when $A(s)$ is large to

$$\frac{V_{out}}{V_{in}} \approx -\frac{R_2}{R_1}\frac{1}{1 + \frac{s}{\frac{1}{R_2C_1}}} \tag{3.4}$$

Hence, a lossy integrator.

b) The transfer function of the circuit can be written in the form

$$H(s) = K\frac{A(s)}{1 + \beta(s)A(s)} \tag{3.5}$$

derive the feed back factor $\beta(s)$.

The β can be derived using several approaches. Either by converting the expression in Eq. (3.3) into the form of Eq. (3.5) or by using the fact that the β factor is the part of the output voltage that is fed back to the input of the operational amplifier. Here we derive the feed back factor by the latter approach.

Break the feedback loop to the right of C_1 and R_2 and compute the transfer function to the input of the OPamp when the input is grounded.

$$\beta(s) = \frac{R_1}{R_1 + R_2 \parallel sC_1} = \frac{R_1}{R_1 + \frac{R_2\frac{1}{sC_1}}{R_2 + \frac{1}{sC_1}}} = \frac{R_1(1 + sR_2C_1)}{R_1 + R_2 + R_1R_2sC_1}$$

c) Derive the transfer function of the building block when $A(s) \to \infty$

This transfer function is found utilizing the expression in Eq. (3.3).

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}\frac{1}{1 + \frac{s}{\frac{1}{R_2C_1}}} \tag{3.6}$$

which is a lossy integrator.

4. Switched-capacitor circuit analysis

a) Compute the output voltage in the Z-domain.

The negative plate of the capacitors are assumed to be connected to the input of the active device (OTA). In the first clock cycle we have that

$q_1(t) = V_1(t)C_1$, $q_2(t) = C_2V_{out}(t)$.

In the clock cycle $t + \tau$

$q_1(t+\tau) = C_1V_2(t+\tau)$, $q_2(t+\tau) = C_2V_{out}(t+\tau)$.

and in clock cycle $t + 2\tau$

$q_1(t+2\tau) = V_1(t+2\tau)C_1$, $q_2(t+2\tau) = C_2V_{out}(t+2\tau)$.

The charge conservation equations are

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau) \tag{4.1}$$

$$q_2(t+\tau) = q_2(t+2\tau) \tag{4.2}$$

Equation (4.2) yields that $V_{out}(t+2\tau) = V_{out}(t+\tau)$. Further, (4.1) together with the former result yield

$V_1(t)C_1 + C_2V_{out}(t) = C_1V_2(t+\tau) + C_2V_{out}(t+2\tau)$

Some simplifications give

$C_1(V_1(t) - V_2(t+\tau)) = C_2(V_{out}(t+2\tau) - V_{out}(t))$. Further, we know that $V_2(t) = V_2(t+\tau)$.

Hence, $C_1(V_1(t) - V_2(t)) = C_2(V_{out}(t+2\tau) - V_{out}(t))$.

Performing a Z transformation yields

$C_1(V_1(z) - V_2(z)) = V_{out}(z)C_2(z-1)$

and the output voltage is expressed as

$$V_{out}(z) = \frac{C_1}{C_2}\left(\frac{V_1(z) - V_2(z)}{z-1}\right) \tag{4.3}$$

Hence, the circuit is a differential accumulator.

b) Is the circuit insensitive to parasitics?

The circuit together with the parasitics introduced by the switches and the

top and bottom plate is shown in

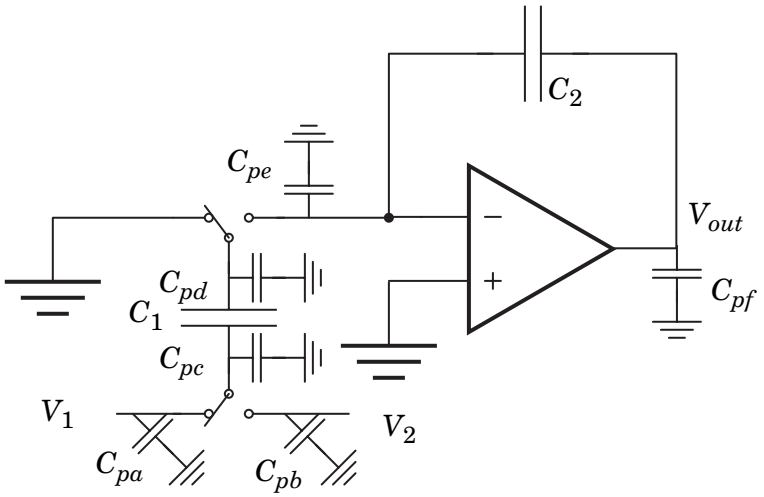

Figure 4.1 SC circuit with capacitive parasitics.

C_{pa} and C_{pb} does not change the transfer function since it is connected to the input sources.

C_{pc} Is charged in clock phase 1 and charged/discharged in clock phase 2, not changing the transfer function.

C_{pd} Connected between ground and ground or ground and virtual ground not changing the transfer function.

C_{pe} Connected between virtual ground and ground and thereby not changing the transfer function.

C_{pf} connected between ground and to the output of the amplifier. Hence not changing the transfer function.

The circuit is insensitive to capacitive parasitics.

c) The amplifier has a finite gain, A. Derive the output voltage, $V_{out}(z)$, for clock phase 1.

Charge conservation is used in order to define the output voltage as a function of the input voltages. The output voltage of the amplifier is $V_{out} = A(V_p - V_n) = A(-V_n)$ which yields that $V_n = -V_{out}/A$ in both clock phases.

$q_1(t) = V_1(t)C_1$, $q_2(t) = C_2(V_{out}(t) + V_{out}(t)/A)$.

In the clock cycle $t + \tau$

$q_1(t + \tau) = C_1(V_2(t + \tau) + (V_{out}(t + \tau)/A))$,
$q_2(t + \tau) = C_2(V_{out}(t + \tau)(1 + 1/A))$.

and in clock cycle $t + 2\tau$

$q_1(t + 2\tau) = V_1(t + 2\tau)C_1$, $q_2(t + 2\tau) = C_2 V_{out}(t + 2\tau)(1 + 1/A)$.

The charge conservation equations are

$$q_1(t) + q_2(t) = q_1(t + \tau) + q_2(t + \tau) \tag{4.4}$$

$$q_2(t + \tau) = q_2(t + 2\tau) \tag{4.5}$$

Equation (4.2) yields that $V_{out}(t + 2\tau) = V_{out}(t + \tau)$. Further, (4.1) together with the former result yield

$V_1(t)C_1 + C_2 V_{out}(t)\left(1 + \frac{1}{A}\right) =$

$C_1(V_2(t) + (V_{out}(t+2\tau)/A)) + C_2V_{out}(t+2\tau)(1+1/A)$
Some simplifications give
$C_1(V_1(t) - V_2(t)) = C_2(V_{out}(t+2\tau) - V_{out}(t))\left(1+\frac{1}{A}\right) + \frac{C_1V_{out}(t+2\tau)}{A}$.
Performing a Z transformation yields
$C_1(V_1(z) - V_2(z)) = V_{out}(z)C_2(z-1)\left(1+\frac{1}{A}\right) + C_1V_{out}(z)\frac{z}{A}$
and the output voltage is expressed as

$$V_{out}(z) = \frac{C_1}{C_2}\left(\frac{V_1(z)-V_2(z)}{\left(1+\frac{1+C_1/C_2}{A}\right)z + \left(1+\frac{1}{A}\right)}\right) =$$

$$= \frac{C_1}{C_2\left(1+\frac{1+C_1/C_2}{A}\right)}\left(\frac{V_1(z)-V_2(z)}{z - \frac{(A+1)C_2}{(A+1)C_2+C_1}}\right) \qquad (4.6)$$

Hence, the circuit is a differential accumulator with loss.

5. A mixture of questions

a) Derive the common-mode and output ranges of the circuit.

The minimum input voltage is determined from all paths from ground to the input. Hence,

$$V_{cm,min} = V_{DS,sat7} + V_{GS1} = \sqrt{\frac{I_{D7}}{\alpha_7}} + \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{T1} \qquad (5.1)$$

The maximum input voltage is

$$V_{cm,max} = V_{DD} - V_{SG5} - V_{SG3} - V_{DS,sat1} + V_{GS1} =$$

$$= V_{DD} - \sqrt{\frac{I_{D5}}{\alpha_5}} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T5} - V_{T3} + V_{T1} \qquad (5.2)$$

The output range is determined by

$$V_{out,min} = V_{DS,sat7} + V_{DS,sat2} = \sqrt{\frac{I_{D7}}{\alpha_7}} + \sqrt{\frac{I_{D2}}{\alpha_2}} \qquad (5.3)$$

and the output range is

$$V_{out,max} = V_{DD} - V_{SG5} - V_{SG3} + V_{SG4} - V_{SD,sat4} =$$

$$= V_{DD} - \sqrt{\frac{I_{D5}}{\alpha_5}} - V_{T5} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T3} + V_{T4} \qquad (5.4)$$

b) Derive the differential and the common-mode output voltage. From your result, what are the benefits of using fully differential compared to single-ended structures?

The differential output voltage is described by

$$V_{out,\,diff} = V_{out,\,p} - V_{out,\,n} = (a_p + a_n)V_{in,\,diff} + (b_p - b_n)V_{in,\,diff}^2 + (c_p + c_n)V_{in,\,diff}^3$$

where $a_p \approx a_n$, $b_p \approx b_n$, and $c_p \approx c_n$. The common-mode output is given by

$$V_{out,\,cm} = \frac{V_{out,\,p} + V_{out,\,n}}{2} = \frac{(a_p - a_n)}{2}V_{in,\,cm} + \frac{(b_p + b_n)}{2}V_{in,\,cm}^2 + \frac{(c_p - c_n)}{2}V_{in,\,cm}^3$$

The fully differential circuit we see that the even-order distortion terms are small for the differential output voltage compare to a single-ended structure (where the output voltage is described by the expression $V_{out} = a_p(V_{in,\,p} - V_{in,\,n}) + b_p(V_{in,\,p} - V_{in,\,n})^2 + c_p(V_{in,\,p} - V_{in,\,n})^3$). The common-mode voltage is dominated by second-order distortion and by matching errors.

c) In analog circuit design it is not common to use the minimum channel length of the transistors. Give two reasons for this.

Minimum channel length is not commonly used in analog circuit design due to matching reasons of the transistors. Further, a small channel-length also increases the channel-length modulation. Hence, decreased output impedance and DC gain of the CMOS circuits.