Correct(?) Solutions to Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	March 13, 2002
Time:	8 - 12
Place:	Kårallen and U6
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

This exam covers nearly the whole course except the filter chapters. Our advise to you is to start by reading through the exam and then begin to solve the exercises that you are familiar with.

Exercise

1. Basic CMOS building blocks

a and b) Sketch the output voltage as a function of the power supply voltage when V_{DD} ramps from 0 to 5 threshold voltages. The input DC voltage $V_{in} = V_{DD}/2$ with a small signal variation.

The output voltage is given by the expression

$$V_{out} = V_{DD} - RI \tag{1.1}$$

where the current I is defined by the transistor. We know that an NMOS transistor is operating in the cut-off region when the gate source voltage is lower than the threshold voltage of the transistor. In this case the transistor must have a power supply voltage smaller than $2V_T$ to ensure that the transistor is operating in the cut-off region. When the transistor is in cut-off the current through the transistor will be close to zero. The output voltage will then be equal to the power supply voltage. Hence, the output voltage increases linearly with V_{DD}.

A further increase of the power-supply voltage will result in a transistor operating in the saturation region since $V_{ds} > V_{gs} - V_T > 0$ so the current through the transistor will start to increase quadratically with increased power supply voltage and thereby decreasing the output voltage quadratically.

For a special input voltage, i.e., $V_{ds} = V_{gs} - V_T > 0$ the transistor will start to operate in the linear region. Hence the output voltage will decrease linearly with increased power supply voltage. To compute when the transistor starts to operate in the linear region we start by defining the current through the transistor in the saturation region.

$$I = \alpha\left(\frac{V_{DD}}{2} - V_T\right)^2 \tag{1.2}$$

where the channel length modulation is ignored. Inserting Eq. (1.2) in Eq. (1.1) gives the following expression

$$V_{out} = V_{DD} - R\alpha\left(\frac{V_{DD}}{2} - V_T\right)^2 \tag{1.3}$$

The transition from the linear to the saturation region occurs when

$$V_{out} = \frac{V_{DD}}{2} - V_T \tag{1.4}$$

Inserting this into Eq. (1.3) and solve for V_{DD} gives:

$$V_{DD} = 2V_t + \frac{1}{\alpha R} + \frac{1}{\alpha R}\sqrt{1 + 8\alpha R V_T} \tag{1.5}$$

The output voltage as a function of the power supply voltage is shown in

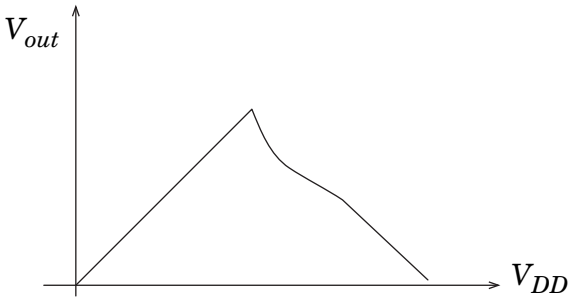

Figure 1.1 The output voltage as a function of the power supply voltage.

c) State two reasons why we seldomly use amplifiers with resistive load in analog integrated circuits.

We do not like to have resistive load in analog circuit because we can only achieve low gain circuits.

Another explanation is the large chip area it will occupy and the large parasitics associated with the large area.

2. Small signal analysis

Assume that all transistors are biased so that they are operating in the saturation region.

a) Derive the small signal transfer function from the input to the output. All parasitics except the source gate capacitor of transistor M_3 can be neglected. Express the DC-gain and the poles of the circuit.

The equivalent small signal scheme for the folded cascode amplifier is shown in

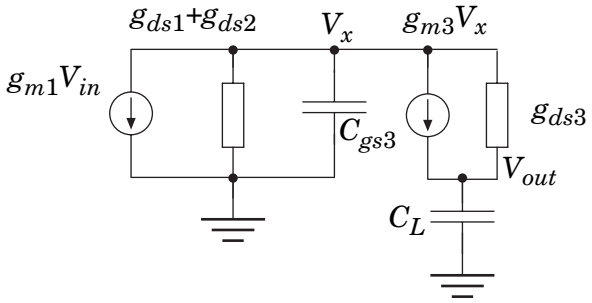

Figure 2.1 The small signal scheme of a folded cascode amplifier.

Using nodal analysis in the nodes V_x and V_{out} yields the following equations

$$g_{m1}V_{in} + V_x(g_{ds1} + g_{ds2} + sC_{gs3}) + g_{m3}V_x + (V_x - V_{out})g_{ds3} = 0 \tag{2.1}$$

$$g_{m3}V_x + (V_x - V_{out})g_{ds3} - V_{out}sC_L = 0 \tag{2.2}$$

Solving for V_x in Eq. (2.2) gives and expression for V_x as a function of V_{out}

$$V_x = \frac{g_{ds3} + sC_L}{g_{m3} + g_{ds3}}V_{out} \tag{2.3}$$

Inserting this equation into Eq. (2.1) gives the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{\frac{(g_{ds1} + g_{ds2})g_{ds3}}{g_{m3} + g_{ds3}} + s\left(C_L\left(1 + \frac{g_{ds1} + g_{ds2}}{g_{m3} + g_{ds3}}\right) + C_{gs3}\frac{g_{ds3}}{g_{m3} + g_{ds3}}\right) + s^2\frac{C_L C_{gs3}}{g_{m3} + g_{ds3}}}$$

The DC-gain can be expressed as

$$A_0 = \frac{g_{m1}}{\frac{(g_{ds1} + g_{ds2})g_{ds3}}{g_{m3} + g_{ds3}}} \tag{2.4}$$

The poles can be approximated by the following formula

$$\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) \approx 1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{2.5}$$

which yields

$$p_1 \approx \frac{\dfrac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}+g_{ds3}}}{C_L\left(1+\dfrac{g_{ds1}+g_{ds2}}{g_{m3}+g_{ds3}}\right)} \approx \frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}C_L} \tag{2.6}$$

and

$$p_2 \approx \frac{1}{C_{gs3}}(g_{m3}+g_{ds3}+g_{ds1}+g_{ds2}) \approx \frac{g_{m3}}{C_{gs3}} \propto \frac{\sqrt{\frac{W_3}{L_3}I_{D3}}}{W_3 L_3} \tag{2.7}$$

$$\omega_u \approx A_0 p_1 \approx \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\frac{W_1}{L_1}I_{D1}}}{C_L} \tag{2.8}$$

b) Describe two ways to increase the phase margin. What will happen to the other performance parameters?

The phase margin is increased if the second pole is move further away from the unity-gain frequency.

This can be achieved by decreasing the transconductance of transistor M_1 by decreasing the width of M_1 or the current through M_1. Which decreases and increases the DC-gain respectively.

Another way is to hold the unity-gain frequency still while the second pole is moved towards high frequencies. This can be done by decreasing the width of transistor M_3 which decreases the gate source capacitance linearly and increases the transconductance by the power 0.5. The DC gain will decrease and the first pole will increase.

c) What is the range of the possible values for V_{bias2} to ensure that all transistors are operating in the saturation region

The maximum voltage to insure that all transistors are operating in the saturation region is restricted by

$$V_{DD} - V_{sd2sat} - V_{sg3} = V_{DD} - \sqrt{\frac{I_{D2}}{\alpha_2}} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T3} \tag{2.9}$$

The minimum output voltage is in this case equal to ground. The minimum bias voltage is then

$$0 + V_{sdsat} - V_{sg} = -V_{T3} \tag{2.10}$$

or

$$V_{in} - V_{T1} - V_{T3} \tag{2.11}$$

depending on the input voltage.

3. Operational amplifier

We have designed the following OTA. All transistors are operating in the saturation region. The transfer function is given by

$$A(s) = \frac{\frac{g_{m8}}{g_{m4}}\frac{g_{m1}}{\frac{g_{ds8}g_{ds10}}{g_{m10}} + \frac{g_{ds12}g_{ds14}}{g_{m12}}}}{1 + \frac{sC_L}{\frac{g_{ds8}g_{ds10}}{g_{m10}} + \frac{g_{ds12}g_{ds14}}{g_{m12}}}} \tag{3.1}$$

No capacitive parasitics are taken into account.

a) Derive the common-mode and output ranges. Use relevant design parameters such as I, W, and L.

The minimum possible input voltage is

$$V_{inmin} = V_{ds5,\,sat} + V_{gs1} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{T1} \tag{3.2}$$

The maximum possible input voltage is

$$V_{inmax} = max\{V_{DD} - V_{sd3,\,sat} - V_{sd7,\,sat} - V_{ds1,\,sat} + V_{gs1},\, V_{DD} - V_{sg3} - V_{ds1,\,sat} + V_{gs1}\}$$

$$= max\left\{V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} - \sqrt{\frac{I_{D7}}{\alpha_7}} + V_{T1},\, V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T3} + V_{T1}\right\}$$

$$CMR = [V_{inmin}, V_{inmax}] \tag{3.3}$$

The maximum possible output voltage is

$$V_{outmax} = V_{DD} - V_{sd8,\,sat} - V_{sd10,\,sat} = V_{DD} - \sqrt{\frac{I_{D8}}{\alpha_8}} - \sqrt{\frac{I_{D10}}{\alpha_{10}}} \tag{3.4}$$

The minimum possible output voltage is

$$V_{outmin} = V_{ds14,\,sat} + V_{ds12,\,sat} = \sqrt{\frac{I_{D14}}{\alpha_{14}}} + \sqrt{\frac{I_{D12}}{\alpha_{12}}} \tag{3.5}$$

$$OR = [V_{inmin}, V_{outmax}] \tag{3.6}$$

b) State two ways to increase the output resistance of the circuit?

The output conductance is given by the expression

$$\frac{g_{ds8}g_{ds10}}{g_{m10}} + \frac{g_{ds12}g_{ds14}}{g_{m12}} \propto \frac{\lambda_p^2 I_{D8}^2}{\sqrt{W_{10} I_{D8}}} + \frac{\lambda_n^2 I_{D8}^2}{\sqrt{W_{12} I_{D8}}} \tag{3.7}$$

The output resistance is increased if the output conductance is decreased. The conductance is decreased if the currents through the output stage I_{D8} is decreased or by increasing the widths of M_{10} or M_{12}. There are also other ways to increase the phase margin.

c) This circuit is not the best circuit to be used when we like to drive small resistive load. Why?

We will have some problems with the operation point of the amplifier since the output resistance will be connected in parallel with the load resistor and thereby changing the operation point. Furthermore we will have decreased output resistance and thereby decreased DC gain.

d) Assume that the amplifier is a one pole system according to the following

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} \tag{3.8}$$

Derive the expression for the unity-gain frequency. What will the DC gain be of closed loop system if the feedback factor $\beta = 0.5$ if $A_0 \gg 1$?

The unity-gain frequency is defined as the frequency where we have a gain equal to unity, $|A(j\omega_u)| = 1$

$$\left| \frac{A_0}{1 + \frac{j\omega}{p_1}} \right| = \frac{A_0}{\sqrt{1 + \frac{\omega^2}{p_1^2}}} = 1 \tag{3.9}$$

Solving for ω gives $\omega_u = \sqrt{(A_0^2 - 1)p_1^2}$. The transfer function of a closed loop system is given by

$$\left. \frac{A(s)}{1 + \beta A(s)} \right|_{s=0} = \frac{A_0}{1 + \beta A_0} = \frac{1}{\beta + \frac{1}{A_0}} \approx \frac{1}{\beta} = 2 \tag{3.10}$$

4. Switched capacitor

a) Derive the transfer function for the switched capacitor circuit, i.e., $V_2(z)/V_1(z)$. Assume that the OTA is ideal.

The circuit in the two different clock cycles is shown in

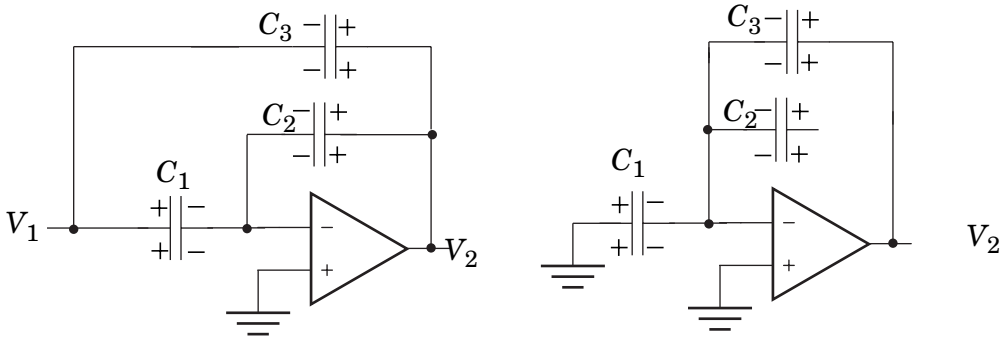

Figure 4.1 The circuit in both clock cycles.

Charge analysis

time t:

$$q_1(t) = C_1 V_1(t),\ q_2(t) = C_2 V_2(t),\ q_3(t) = C_3(V_2(t) - V_1(t)), \tag{4.1}$$

time t+τ:

$$q_1(t+\tau) = 0,\ q_2(t+\tau) = q_2(t),\ q_3(t+\tau) = C_3 V_2(t+\tau) \tag{4.2}$$

q_2 will keep its charge since it is connected only to one terminal.

time t+2τ:

$$q_1(t+2\tau) = C_1V_1(t+2\tau),\ q_2(t+2\tau) = C_2V_2(t+2\tau),$$
$$q_3(t+2\tau) = C_3(V_2(t+2\tau) - V_1(t+2\tau)) \tag{4.3}$$

The charge conservation equations are

$$q_1(t) + q_2(t) + q_3(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{4.4}$$

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) \tag{4.5}$$

Using Eq. (4.4) together with the expression above gives:

$$C_1V_1(t) + C_2V_2(t) + C_3(V_2(t) - V_1(t)) = C_2V_2(t) + C_3V_2(t+\tau) \tag{4.6}$$

The Eq. (4.5) gives the following expression

$$C_2V_2(t) = C_1V_1(t+2\tau) + C_2V_2(t+2\tau) \tag{4.7}$$

computing the transfer function for clock cycle 1 (t, t+2τ, ...) can be done by just taking the Z transform of Eq. (4.7).

$$\frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2}\frac{z}{z-1} \tag{4.8}$$

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.
The circuit with all parasitics is shown in Figure 4.2.

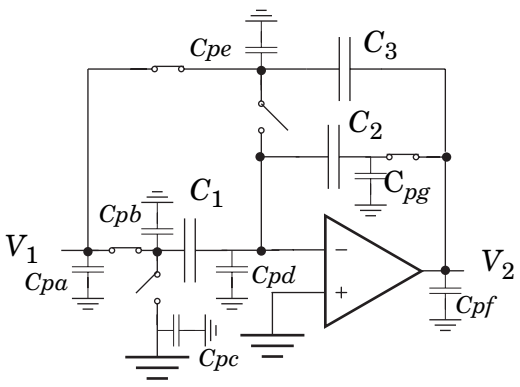

Figure 4.2 The SC circuit with capacitive parasitics.

C_{pa} is connected to the input source which is assumed to be ideal thereby not changing the transfer function.

C_{pb} is connected to the input source or with both pins connected to ground, not changing the transfer function,

C_{pc} Not changing the transfer function since it is connected to ground with both terminals.

C_{pd} Not changing the transfer function since it is connected to ground and virtual ground with the terminals.

C_{pe} in clock phase 1 it is charged to V_1. In the next clock cycle it will

discharge and thereby adding charge to the capacitors C_1, C_2, and C_3.
C_{pf} is connected to the ideal OTA output which does not change the transfer function.
C_{pg} During clock phase 1 C_{pg} will be charged to the output voltage. In clock phase 2 will the charges of capacitor C_2 and C_{pg} not be changed since we have two capacitor connected in parallel with there charges in equilibrium.
Hence, the circuit is sensitive to capacitive parasitics.

c) Assume that the OTA suffers from an input offset voltage, V_{os}. Derive the output voltage $V_{out}(z)$ for the times t, $t + 2\tau$, $t + 4\tau$ and so on.
Charge analysis
time t:

$$q_1(t) = C_1(V_1(t) - V_{os}),\ q_2(t) = C_2(V_2(t) - V_{os}),$$
$$q_3(t) = C_3(V_2(t) - V_1(t)), \tag{4.9}$$

time t+τ:

$$q_1(t+\tau) = C_1(0 - V_{os}),\ q_2(t+\tau) = q_2(t),$$
$$q_3(t+\tau) = C_3(V_2(t+\tau) - V_{os}) \tag{4.10}$$

time t+2τ:

$$q_1(t+2\tau) = C_1(V_1(t+2\tau) - V_{os}),\ q_2(t+2\tau) = C_2(V_2(t+2\tau) - V_{os}),$$
$$q_3(t+2\tau) = C_3(V_2(t+2\tau) - V_1(t+2\tau)) \tag{4.11}$$

The charge conservation equations are

$$q_1(t) + q_2(t) + q_3(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{4.12}$$

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) \tag{4.13}$$

The Eq. (4.13) gives the following expression

$$-C_1V_{os} + C_2(V_2(t) - V_{os}) = C_1(V_1(t+2\tau) - V_{os}) + C_2(V_2(t+2\tau) - V_{os})$$

computing the transfer function for clock cycle 1 (t, t+2τ, ...) can be done by just taking the Z transform.

$$\frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2}\frac{z}{z-1} \tag{4.14}$$

The circuit is insensitive to offset voltages.

5. A mixture of questions

a) What is the difference between an operational amplifier and a operational transconductance amplifier?

An operational amplifier can drive resistive load since it has low output resistance and generates an output voltage that is proportional to the input voltage.

The OTA is not capable to drive low resistive load since it has high output resistance but can drive capacitive load.The output is a current proportional to the input voltage.

b) Why do we like to bias all transistors so that they are operating in the saturation region?

A process variation in the saturation region that changes the drain source voltage does not effect the transfer function directly. Furthermore, the transconductance value of the transistor is high and thereby high gain circuit can be achieved.

c) Explain advantages and drawback of an active-RC integrator compared to a switched capacitor accumulator.

An active-RC integrator is a continuos-time integrator and it can handle signals with high bandwidth. The problem is the value of the time constants $1/(RC)$ which is sensitive to process variations.

A switched capacitor accumulator on the other hand can handle signals with lower bandwidth. The time constants is defined by the ratio of two or more capacitors and tight matching can be achieved.

d) What is transistor matching? Describe two ways to increase the matching between two transistors.

Two transistor that is matched will vary nearly equal to process variations, temperature effect and ageing. Improved matching can be achieved by placing two transistors close to each other. Other ways is to divide larger transistors into several unit-size transistors. These unit-sized transistors can be laid out in a interdigitized or common centriod pattern.

e) The circuit shown in Figure 5.1a can be enhanced as shown in Figure 5.1b, how is the performance affected in Figure 5.1b compared to Figure 5.1a (gain, poles and zeroes)?.

The circuit in figure b is a gain boosted version of the cascoded common-source amplifier. This is used when higher DC gain is needed. The first pole is moved to lower frequencies while the other is not changed. More poles and zeros are also introduced in the gain boosting circuit.

f) Linus need to design a circuit with high gain. He have studied bipolar circuit and the gilbert amplifier is a common way to increase the gain of the circuit. He is asking you if the circuit can be designed to have high gain. What would your recommendation be?

Transistor M_1 does not have a DC path to ground. Since the input resistance of transistor M_2 is very high no current will flow through transistor M_1 and thereby no (or very small) gain will be achieved.