TSEI12, Analog Design, Second course, 2013-08-26

Written exam, TEN1

Date, time	**2013-08-26, 08.00 - 12.00**
Location(s)	TER1
Responsible teacher	J Jacob Wikner, 070-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ✗ *Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" clear derivations are understood (and not only text). Note that the questions in the exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ✗ *Notice that even though you may not fully know the answer, add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available within two weeks from exam date (hopefully...)

Table of Contents

1. CMOS, ETC. (5 P)

Consider the circuit in Figure 1.1 below. Derive, explain, and elaborate on the following:

1) The good-old story: Output impedance, DC gain, bandwidth, unity-gain frequency, i.e., the transfer function with identified components.

2) Now, when you did 1) why not present an AC signal schematic

3) Sketch the DC transfer characteristics as a function of V_{in}. Indicate important break points in the graph. Indicate operating regions for the two transistors across the voltage ranges.

4) In 3) - where do you want to put the DC operating point?

Assume all transistors operate in their saturation regions.

- *Minimize the number of parameters in your solutions and use large-signal parameters.*
- *Make valid assumptions and **motivate them well**.*
- *Illustrate your results with example values (e.g. in Volts) and diagrams.*

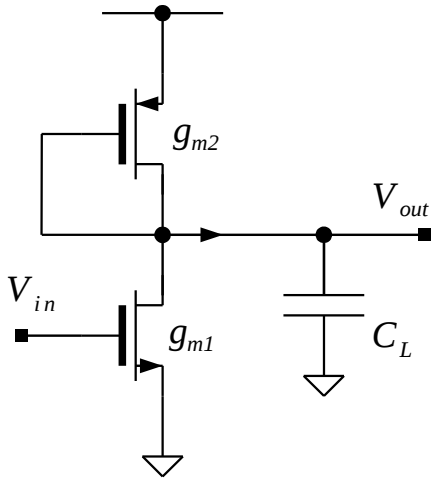

Figure 1.1: Some circuit with some stuff connected to it.

- *This exercise will show that you have understood basic operation regions. Obtainable voltage swings for a CMOS circuit, etc.*
- *Utilize any symmetry in the design!*
- *Did you motivate all the assumptions well?!*

2. NOISE (5 P)

Consider the two circuits in Figure 2.1. All components that can be noisy are noisy. The noise of the operational amplifier(s) has been indicated in the figure - assume it is a constant, $v_n^2(f)=v_{n0}^2$.

1) Derive compact expressions of the **total output noise power** for both circuits.

2) Which one of the two circuits is the **more noisy one**? What assumptions have you made in order to make the conclusion?

Make valid assumptions and motivate them well! Illustrate your results by sketching the corresponding PSD in different steps of your solutions.

- ***Finding a compact expressions implies in this context: "Minimize the number of design parameters in your expression."***

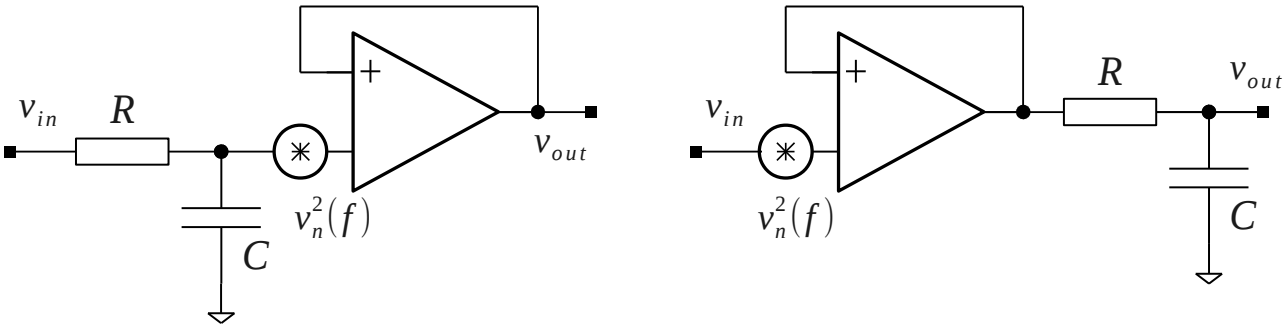

Figure 2.1: A buffer and some passive circuit.

- *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth:* $p_1/4$.
- *What assumptions can you do about the opamp bandwidth to simplify your noise calculations?*
- *The noise voltage of a resistance is* $v_R^2(f)=4kTR$

3. OP/OTA, STABILITY (5 P)

Consider the configuration in Figure 3.1. There are two amplifiers in series, the output conductance of the first stage is G_I, and for the second it is G_{II}. The transconductances of the respective cases are indicated in the figure.

The total DC voltage gain is 7200 and the DC gain of the second stage is eight times the gain of the first stage.

1) What is the total transfer function of the system?

2) Assume well-separated poles: As a function of C_I, what values can the load capacitance C_{II} take to guarantee a 45-degree phase margin?

Your answers should of course be supported by diagrams as well as formulas.

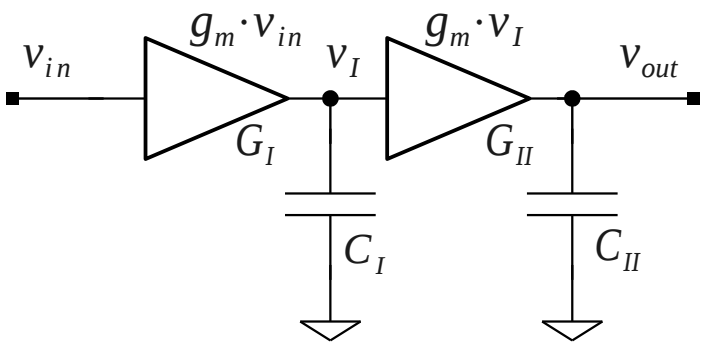

Figure 3.1: A two-stage amplifier.

- *And once again! Do not forget to present your results properly!*
- *Notice that you have quite some help in the handouts from the course...*

4. TRANSMISSION LINES (5 P)

Consider the circuit in Figure 4.1. It has a transmitter and a receiver on two chips. The transmission line is on a PCB with a good ground plane. The transmitter has an output resistance of R_{out} and the receiver has an input resistance of R_{in}. The transmission line has a characteristic impedance of Z_0. The length of the line is 5 cm, and the propagation speed through the line is $v = 2 \cdot 10^8$ m/s.

Further on, we also know that: $R_{out} = 25$ Ohm, $Z_0 = 50$ Ohm, and $R_{in} = 75$ Ohm. The transmitter will ideally output 1-V voltage pulses with a very short rise/fall time, internally.

1) Once the pulses start to be transmitted over the line, sketch the diagram showing the voltage at the receiver input **as function of time.**

2) What are the reflection constants at the receiver and transmitter?

You are allowed to modify the PCB in a way that you can add termination in series and parallel.

3) Modify the PCB such that you have maximum power transfer from the transmitter to the receiver.

4) Modify the PCB such that you have a minimum number of reflected waves traveling back-and-forth.

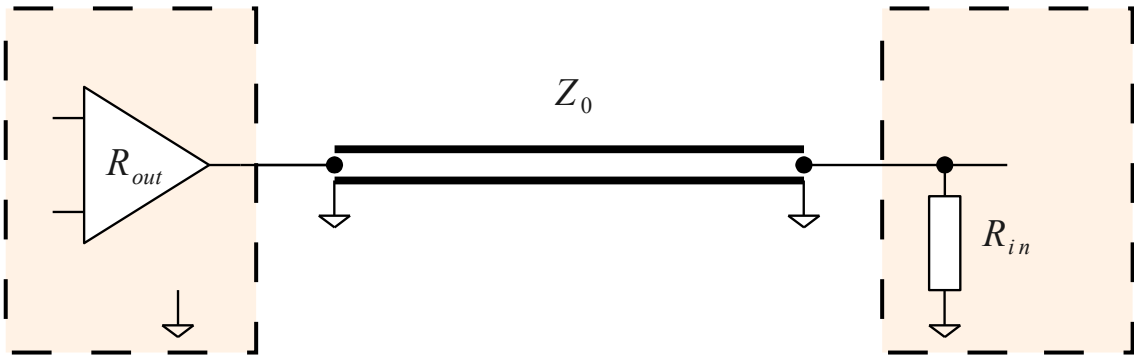

Figure 4.1: A circuit communicating with another circuit over a transmission line.

✗ *Just use approximate values... and sketch does not mean to draw with infinite accuracy...*

5. POWER SYSTEMS, TIMING, MISC (5 P)

Consider the two decoupling (bypass) capacitors in Figure 5.1. They are typically used to filter out any high-frequency noisy signals along the supply wire. In the figure, we also see the model of the decoupling capacitor with the nonideal components ESR and ESL.

Assume that the nominal capacitance values, C0 and C1, can be different, but that the ESR and ESL are the same for the two capacitors.

1) Sketch the impedance of one capacitor, for example C0, as a function of frequency. Identify any extreme points/characteristics along the curve and explain them.

2) Sketch the impedance of the combined pair of capacitors, i.e., C0 and C1, as a function of frequency. In this part, assume the capacitance in C0 is much smaller than that of C1. Identify any extreme points/characteristics along the curve and explain them.

3) What is the minimum impedance between ground and supply that can be obtained with the two capacitors? When does this happen?

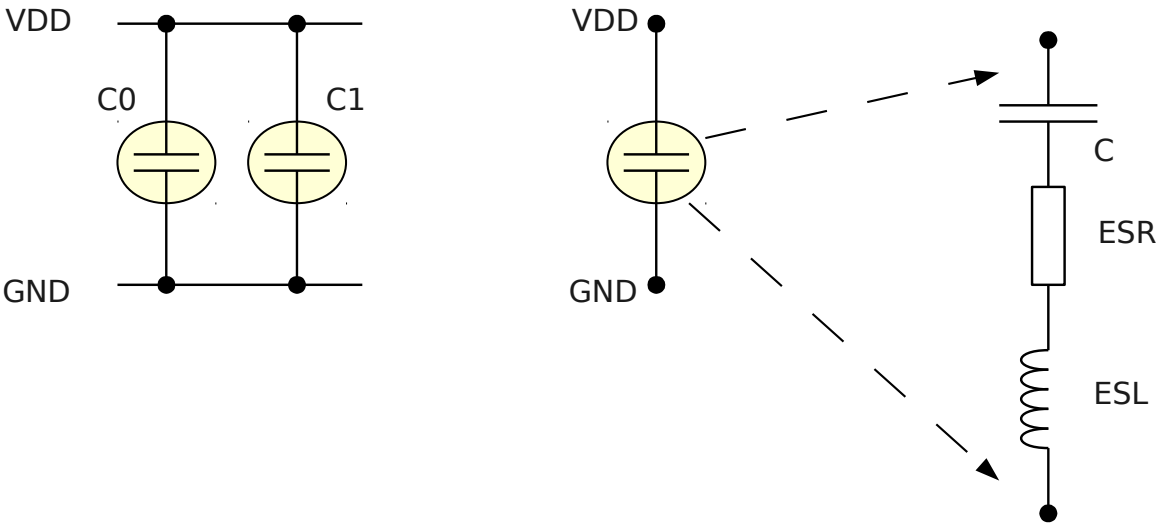

Figure 5.1: Two decoupling capacitors in parallel (left) and their model (right).