SOLUTIONS. Excercise Examination, 2008

TSEI05 Analog and Discrete-time Integrated Circuits.

Excercise 1.

a) A PMOS transistor is saturated when $V_{SD} > V_{eff} = V_{SG} - V_{tp}$.

Transistor **M1**: $V_{SD1} = V_{DD} - V_x = V_{SG1}$ i.e. $V_{SD1} > V_{SG1} - V_{tp1}$, so **M1** works in *saturation*.

Transistor **M2**: $V_{SD2} = V_x - V_{bias} = V_{SG2}$ i.e. $V_{SD2} > V_{SG2} - V_{tp2}$, so **M2** works in *saturation*.

A NMOS transistor is saturated when $V_{DS} > V_{eff} = V_{GS} - V_{tn}$.

Transistor **M3**: $V_{DS3} = V_{bias} - 0 = V_{GS3}$ i.e. $V_{DS3} > V_{GS3} - V_{tn3}$, so **M3** works in *saturation*.

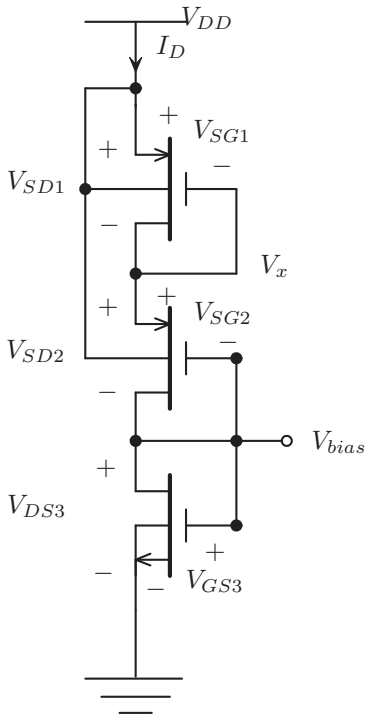

Figure 1: A bias circuit.

b) First note that $I_{D1} = I_{D2} = I_{D3} = I_D$

Transistor **M1**: $V_{SB1} = 0$ i.e. $V_{tp1} = V_{t0p}$.

Enclosed page of formulas gives:

$$\left(\frac{W}{L}\right)_1 = \frac{I_D}{\frac{1}{2}\mu_{0p}C_{oxp}V_{eff1}^2(1+\lambda_p(V_{SD1}-V_{eff1}))} \tag{1}$$

$I_D = 5\ \mu$ A, $\mu_{0p}C_{oxp} = 58.5\ \mu$ A/V^2,

$V_{eff1} = V_{SG1} - V_{t0p} = V_{DD} - V_x - V_{t0p} = 3.3 - 0.6 - 0.62 = 2.08$ **V** ,
$\lambda_p = 0.05$.
Further $V_{SD1} = V_{SG1}$ gives $V_{SD1} - V_{eff1} = V_{t0p} = 0.62$ **V**.
Now equation (1) gives:

$$\left(\frac{W}{L}\right)_1 \approx 0.42 \tag{2}$$

Transistor **M2**: $V_{SB2} = V_{S2} - V_{B2} = V_x - V_{DD} = -1.25$ **V**.

Enclosed page of formulas gives:

$$V_{tp2} = V_{t0p} + \gamma(\sqrt{2\phi_F - V_{SB2}} - \sqrt{2\phi_F}) = 0.62 + 0.41(\sqrt{2.07} - \sqrt{0.82} = 0.8386 \text{ V} \tag{3}$$

$$\left(\frac{W}{L}\right)_2 = \frac{I_D}{\frac{1}{2}\mu_{0p}C_{oxp}V_{eff2}^2(1 + \lambda_p(V_{SD2} - V_{eff2}))} \tag{4}$$

$I_D = 5\ \mu$ **A**, $\mu_{0p}C_{oxp} = 58.5\ \mu$ **A/V**^{2},
$V_{eff2} = V_{SG2} - V_{tp2} = V_x - V_{bias} - V_{tp2} = 2.05 - 0.6 - 0.8386 = 0.6114$ **V** ,
$\lambda_p = 0.05$.
Further $V_{SD2} = V_{SG2}$ gives $V_{SD2} - V_{eff2} = V_{tp2} = 0.8386$ **V**.
Now equation (4) gives:

$$\left(\frac{W}{L}\right)_2 \approx 0.44 \tag{5}$$

Transistor **M3**: $V_{BS3} = 0$ i.e $V_{tn3} = V_{t0n} = 0.47$.

$$\left(\frac{W}{L}\right)_3 = \frac{I_D}{\frac{1}{2}\mu_{0n}C_{oxn}V_{eff3}^2(1 + \lambda_n(V_{DS3} - V_{eff3}))} \tag{6}$$

$I_D = 5\ \mu$ **A**, $\mu_{0n}C_{oxn} = 180\ \mu$ **A/V**^{2},
$V_{eff3} = V_{GS3} - V_{t0n} = V_{bias} - 0 - V_{tp2} = 0.6 - 0.47 = 0.13$ **V** ,
$\lambda_n = 0.03$.
Further $V_{DS3} = V_{GS3}$ gives $V_{DS3} - V_{eff3} = V_{t0n} = 0.47$ **V**.
Now equation (6) gives:

$$\left(\frac{W}{L}\right)_3 \approx 3.24 \tag{7}$$

Answer: $\left(\frac{W}{L}\right)_1 \approx 0.42$, $\left(\frac{W}{L}\right)_2 \approx 0.44$ and $\left(\frac{W}{L}\right)_3 \approx 3.24$

Exercise 2.

Figure 2 gives the complete small signal equivalent circuit (SSEC):
Notice that:

- $V_{gs1} = V_{g1} - V_{s1} = V_{in}$
- $V_{gs2} = V_{g2} - V_{s2} = V_{in}$
- $V_{gs3} = 0 - V_{s3} = -V_x$
- $V_{gs4} = 0 - V_{s4} = -V_y$

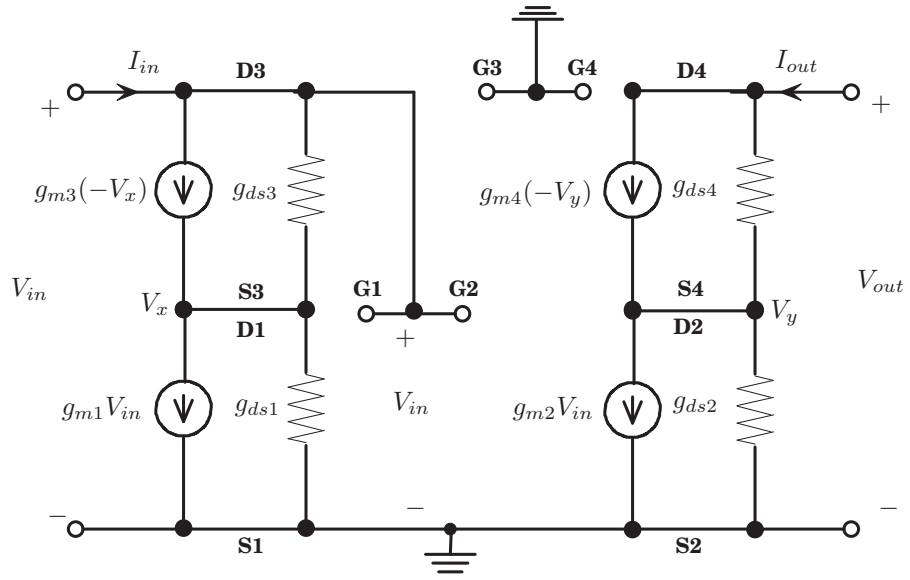

Figure 2: Small signal equivalent circuit.

Determine r_{in}
KCL gives:

$$I_{in} = g_{m3}(-V_x) + (V_{in} - V_x)g_{ds3} \tag{8}$$
$$I_{in} = V_{in}g_{m1} + V_x g_{ds1} \tag{9}$$

Equations (8) and (9) give the input resistance:

$$\underline{\underline{r_{in} = \frac{V_{in}}{I_{in}} = \frac{g_{ds1} + g_{ds3} + g_{m1}}{g_{m1}(g_{ds3} + g_{m3}) + g_{ds1}g_{ds3}}}} \tag{10}$$

Determine r_{out} (OBS! Put V_{in} to zero when calculating r_{out})
KCL gives:

$$I_{out} = g_{m4}(-V_y) + (V_{out} - V_y)g_{ds4} \tag{11}$$
$$I_{out} = V_{in}g_{m2} + V_y g_{ds2} \tag{12}$$

Putting $V_{in} = 0$ gives the output resistans:

$$\underline{\underline{r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds2} + g_{ds4} + g_{m4}}{g_{ds2}g_{ds4}}}} \tag{13}$$

Exercise 3.

a) **Flash ADC:** The reference value on the inverted input of each comparator determins at which level the output from each comparator (totally 7) gives a high voltage.

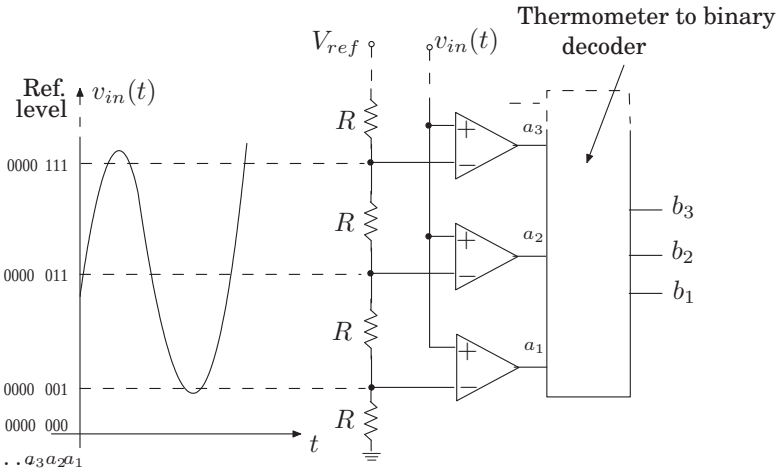

Figure 3: Flash Analog to Digital Converter.

b) **Ideal 3-bit DA-converter:**

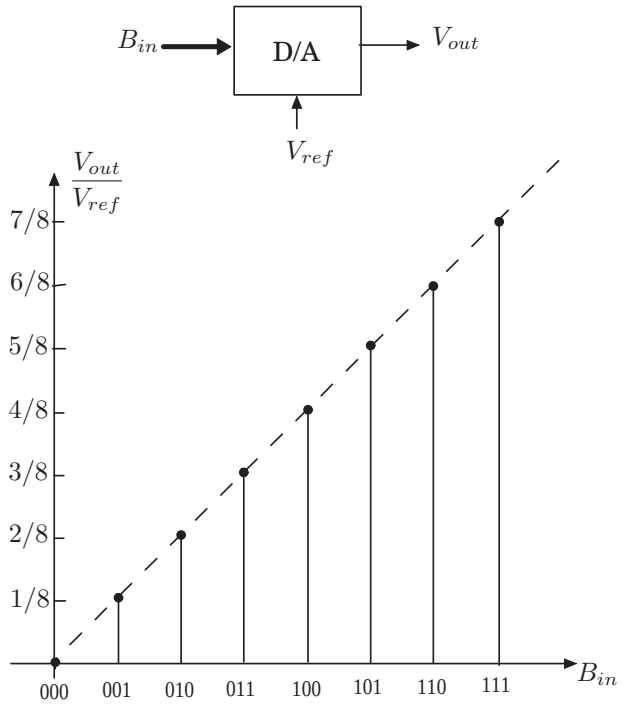

Figure 4: Ideal 3-bit Digital to Analog Converter.

$B_{in} = [1, 0, 1] \Rightarrow V_{out} = \frac{5}{8} \cdot V_{ref} = \frac{10}{8} = 1.25$ V. $\quad V_{LSB} = \frac{1}{8} \cdot V_{ref} = 0.25$ V.

Exercise 4.

Using KCL in node **A** and node **B** respectively in **Figure 5** gives:

$$\textbf{A}: \quad g_{mI}V_{in} + (g_I + sC_I)V_x + sC_c(V_x - V_{out}) = 0 \tag{14}$$

$$\textbf{B}: \quad g_{mII}V_x + (g_{II} + sC_{II})V_{out} + sC_c(V_{out} - V_x) = 0 \tag{15}$$

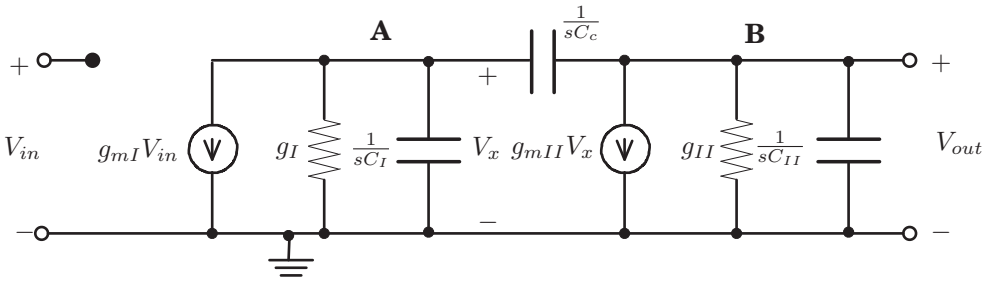

Figure 5: A small-signal model of a two-stage OTA.

Equation (15) gives:

$$V_x = -\frac{g_{II} + sC_{II} + sC_c}{g_{mII} - sC_c} \cdot V_{out} \tag{16}$$

Equation (16) inserted in (14) gives the transfer function:

$$H_(s) = \frac{V_{out}}{V_{in}} = \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + s((C_{II} + C_c)g_I + (C_I + C_c)g_{II} + C_c g_{mII}) + s^2(C_I C_{II} + C_c(C_I + C_{II}))} \tag{17}$$

Exercise 5.

Figure 6a gives a small-signal equivalent circuit, including noise-sources.

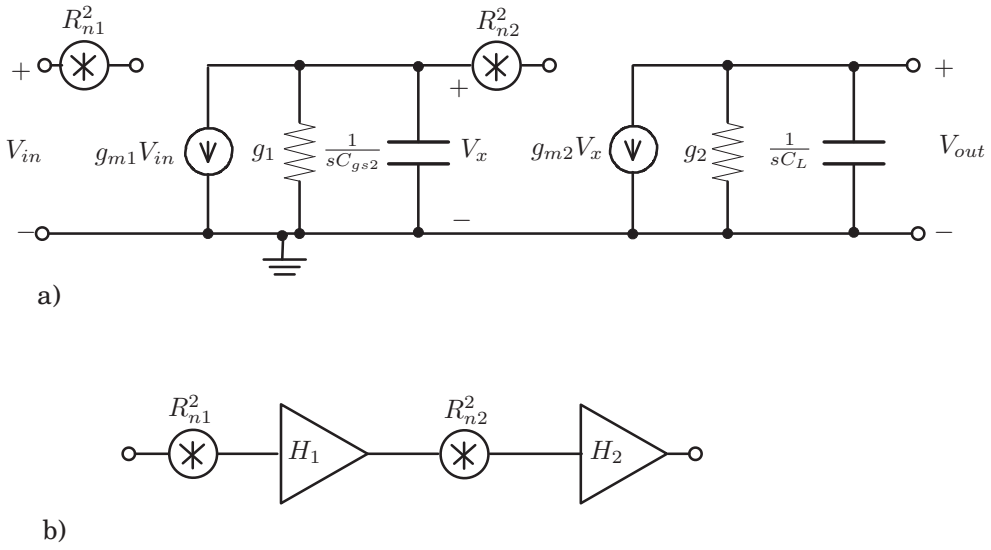

Figure 6: a) A small-signal equivalent. b) Equivalent circuit for determing output noise spectral density

As the noise sources are uncorrelated the output noise spectral density can be computed as **Figure 6b)** discribes, i.e. by the following formula

$$R_{out}(\omega) = |H_1(\omega)|^2|H_2(\omega)|^2 R_{n1}(\omega) + |H_2(\omega)|^2 R_{n2}(\omega) \tag{18}$$

where $H_1(\omega)$ is the transfer function for the first stage and $H_2(\omega)$ the transfer function for the second stage.
From **Figure 6a)** $H_1(s) = V_x(s)/V_{in}(s)$ and $V_x(s) = -g_{m1}V_{in}(s) \cdot \frac{1}{g_{ds1}+sC_{gs2}}$ which yiels

$$H_1(s) = -\frac{g_{m1}}{g_{ds1} + sC_{gs2}} \Rightarrow H_1(\omega) = -\frac{g_{m1}}{g_{ds1} + j\omega C_{gs2}} \tag{19}$$

In the same way $H_2(s)$ is calculated to:

$$H_2(s) = -\frac{g_{m2}}{g_{ds2} + sC_L} \Rightarrow H_2(\omega) = -\frac{g_{m2}}{g_{ds2} + j\omega C_L} \tag{20}$$

Equations (18)-(20) gives following spectral density of the output noise (here we also utilize that $g_{m1} = g_{m2} = g_m$ and $g_{ds1} = g_{ds2} = g_{ds}$):

$$R_{out}(\omega) = R_{n1}(\omega)\frac{g_m^2}{g_{ds}^2 + \omega^2 C_{gs2}^2} \cdot \frac{g_m^2}{g_{ds}^2 + \omega^2 C_L^2} + R_{n2}(\omega)\frac{g_m^2}{g_{ds}^2 + \omega^2 C_L^2} \tag{21}$$

Using that $R_{n1}(\omega) = R_{n2}(\omega) = \frac{8kT}{3}\frac{1}{g_m}$ (from enclosed page of formulas) equation (21) gives:

$$R_{out}(\omega) = \frac{8kT}{3} \cdot \frac{1}{g_m} \cdot \frac{g_m^2}{g_{ds}^2 + \omega^2 C_L^2}\left(\frac{g_m^2}{g_{ds}^2 + \omega^2 C_{gs2}^2} + 1\right) \tag{22}$$

Which gives the answer:

$$\underline{\underline{R_{out}(\omega) = \frac{8kT}{3} \cdot \frac{g_m}{g_{ds}^2 + \omega^2 C_L^2}\left(\frac{g_m^2}{g_{ds}^2 + \omega^2 C_{gs2}^2} + 1\right)}} \tag{23}$$