TSEI05 Analog and Discrete time Integrated Circuits

Exam

Date:	March 13, 2008
Time:	14-18
Place:	TER1
Max.no. of points:	70
Grades:	30p for 3, 15p for 4, and 20p for 5.
Allowed material:	All types of calcuclators except laptops. Formulary.
Examiner:	Sune Söderkvist
Responsible teacher:	Sune Söderkvist. Tel.: 281355.
Corrrect (?) solutions:	Solutions and results will be displayed in House B, entrance 25-27, corridor C ground floor.

Graded exams are returned on examinator's office times, tuesdays and fridays at 11.00-13.00, during week no.45 and 46.

Students instructions

- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

Good Luck!

Exercise 1.

Determine the width-over-length ratios of transistors M1 and M2 in the common drain circuit in **Figure 1**.

$V_{in,DC} = 3$ V, $V_{out,DC} = 1.5$ V, $V_{bias} = 1$ V, $V_{DD} = 3$ V and the current through both transistors are
$I = 20$ nA.

Do not neglect the channel-length modulation nor the body effect.

Constants: $V_{t0} = 0.5$ V, $\mu_0 C_{ox} = 20$ nA/V^2, $\lambda = 0.03$ V^{-1}, $\gamma = 0.6$ V$^{1/2}$ and $\phi_F = 0.4$ V. (5p)

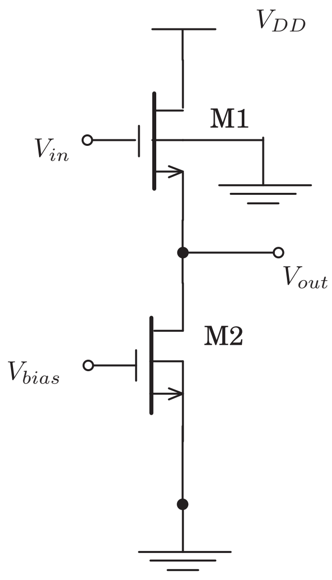

Figure 1: Simple gain-stage.

Exercise 2.

Determine the minimum output voltage V_{out} for the current mirror in **figure 2**. The channel length modulation can be neglected.
The transistors **M3** and **M4** are at the limit of saturation.
Express V_{out} in terms of currents through the transistors and in design parameters α_i, $i = 1, 2, 3, 4, 5, 6$. (Of course constants λ and V_{ti}, $i = 1, 2, 3, 4, 5, 6$ also may be included in the expression for V_{out}.) (5p)

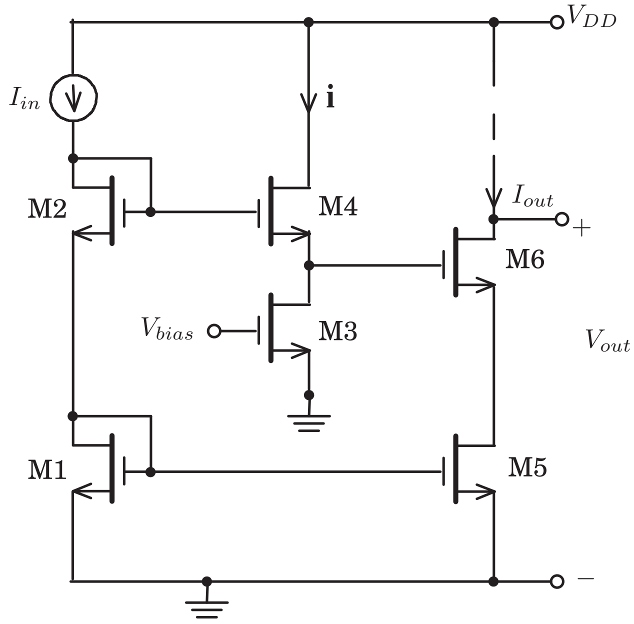

Figure 2: A wide-swing current mirror.

Hint: There are more than one possible path from ground to the output node.

Exercise 3.

a) Sketch a small signal equivalent circuit for the cascode stage in **Figure 3**. (2p)

b) Determine the transfer function $H(s) = V_{out}(s)/V_{in}(s)$ if the parameters of the transistors are g_{m1}, g_{ds1} and g_{m2}, g_{ds2} respectively. The bulk effect can be neglected. (2p)

c) Determine, from the result in b), an approximation for $H(s)$ assuming that $g_{m2} >> g_{ds2}$. From this approximation determine the DC-gain and the unity gain frequency. (1p)

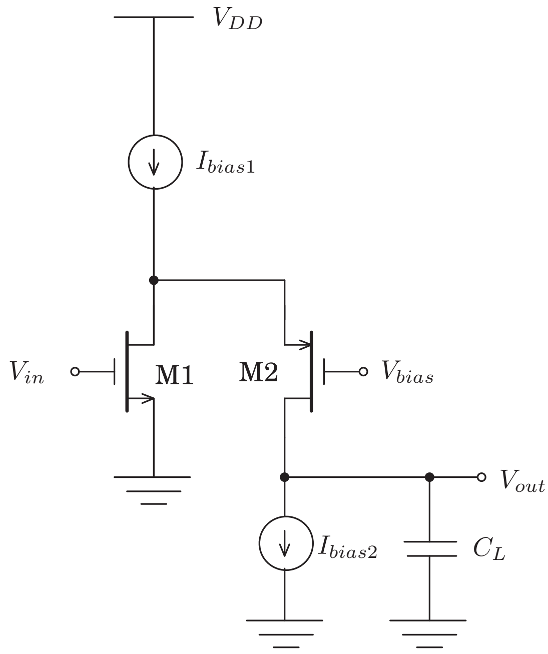

Figure 3: A cascode stage.

Exercise 4.

Sketch a figure that shows the construction of a **resistor-string** DA-converter that converts the binar signal $B_{in} = [b_1, b_2, b_3]$ to an analog signal V_{out}.

Also, describe the function of this DAC by describing how the inputs $B_{in} = [0, 0, 0]$, $B_{in} = [1, 1, 1]$ and $B_{in} = [1, 1, 0]$ affect the transistors. Determine the value of V_{out} when $B_{in} = [1, 1, 0]$, $V_{ref} = 3.2$ V and all resistors $R = 1\ \Omega$. (5p)

Exercise 5.

The inverting amplifier in **Figure 4 a** is used in an application where low noise is of major importance. Hence, a low noise design of the amplifier is required. In this exercise, only the thermal noise in the op.amp. is considered. The gain of the op.amp. $A = g_{m1}/g_{out} = g_{m1}/(g_{ds2} + g_{ds4})$. Further, the ratio between R_2 and R_1 is $R_2/R_1 = a$.

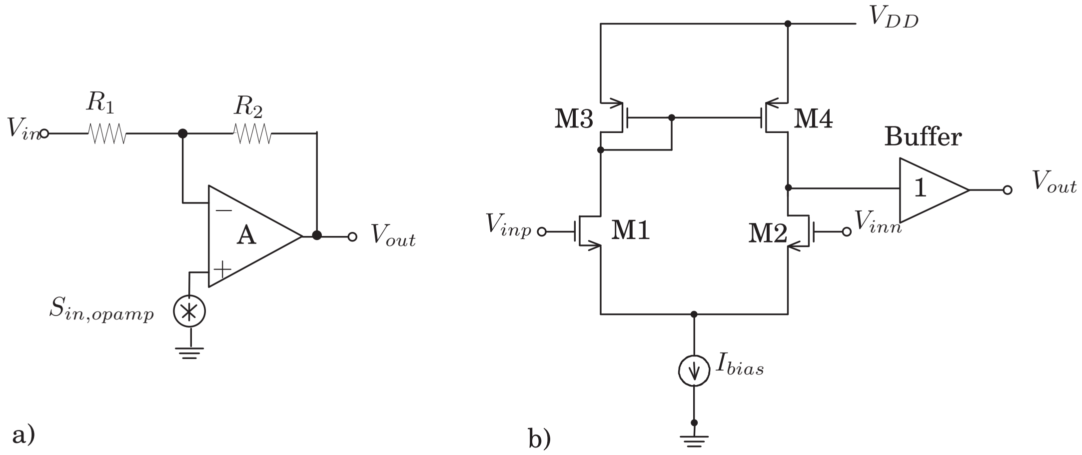

Figure 4: a) A noisy inverting op.amp. b) The principal schematic of the op.amp.

a) Assume that the resistors do not generate any thermal noise while the op.amp. has an equivalent voltage input noise spectral density of

$$S_{in,opamp} = \frac{16kT}{3}\frac{1}{g_{m1}}\left(1 + \frac{g_{m4}}{g_{m1}}\right)$$

where the number in the index refers to the op.amp. implementation in **Figure 4 b**. Compute the equivalent output noise spectral density for the circuit in **Figure 4 a** caused by the noisy amplifier. (4p)

b) State one approach to decrease the equivalent output noise spectral density of the circuit in **Figure 4 a** caused by the operational amplifier. How does this impact the DC gain of the open loop amplifier? (1p)

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_t$	$I_D \approx 0$
Linear:	$V_{GS} - V_t > V_{DS} > 0$	$I_D = \alpha(2(V_{GS} - V_t) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_t < V_{DS}$	$I_D = \alpha(V_{GS} - V_t)^2(1 + \lambda(V_{DS} - V_{eff}))$
	$V_{DSsat} = V_{eff} = V_{GS} - V_t$	
All regions:	$V_t = V_{t,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx 2\alpha V_{DS}$	$g_{ds} \approx 2\alpha(V_{GS} - V_t - V_{DS})$
Saturation:	$g_m \approx 2\sqrt{\alpha I_D}$	$g_{ds} \approx \lambda I_D$

Constants: $\alpha = \frac{1}{2}\mu_{0n}C_{ox}\frac{W}{L}$ $\quad \lambda = \sqrt{\frac{K_s\epsilon_0}{2qN_A\phi_0}} \cdot \frac{1}{L}$ $\quad \gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$R(f) = V^2(f) = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$R(f) = I^2(f) = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$R(f) = V^2(f) = \frac{K}{WLC_{ox}f}$$

Determing noise at the output:

$$R_{out}(f) = \sum_k |H_k(f)|^2 R_{in,k}(f)$$

$$P_{out,noise} = \int_0^\infty R_{out}(f)df$$