VmodTFT™ Reference Manual

Revision: November 11, 2011
Note: This document applies to REV C of the board.

1300 NE Henley Court, Suite 3
Pullman, WA 99163
(509) 334 6306 Voice | (509) 334 6300 Fax

Overview

The VmodTFT board lets you connect an LCD touchscreen to any Digilent FPGA system board with a VHDCI connector. It acts as both an input and output device.

It features a 4.3" wide-format vivid color LED-backlit LCD screen. The screen has a 480×272 native resolution display with a color depth of 24 bits per pixel.

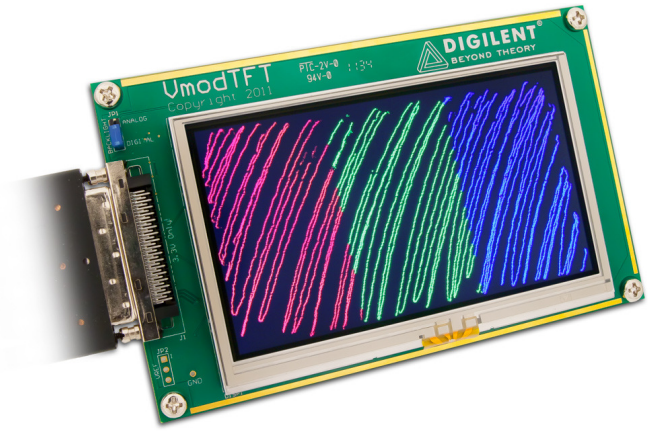
A four-wire resistive touchscreen with anti-glare coating covers the entire active display area.

Features include:

- a 4.3" color TFT LCD with a resistive touchscreen
- 480×272 resolution
- 24 bpp color depth
- 80Hz maximum refresh rate
- an LED backlight with PWM control
- a four-wire resistive touchscreen with an Analog Devices AD7873 touch controller
- 125 kSPS maximum touch sample rate
- an on-board temperature sensor that can detect –40°C to 85°C
- a VHDCI connector

Functional Description

The two-plate four-wire touchscreen uses four analog lines connecting the opposite sides of the X and Y plates. A touch controller gives the touchscreen an FPGA interface. The controller can both drive and sample the touchscreen using a digital serial interface. The LCD is driven using a digital parallel interface.



The LED backlight is driven by the on-board current source. You can change its intensity digitally using a PWM (Pulse Width Modulation) signal or you can set jumper JP1 to analog for the default backlight setting.

The LCD screen and the touchscreen can be used independently. Touch readings are noisier when the LCD is on, but you can filter the noise and still obtain a fast sample rate. If you require maximum precision and sample rates, you should turn the LCD off during touchscreen sampling.

Power-Up Sequence

The LCD has a specific power-up sequence that needs to be followed for proper operation.

The VmodTFT should only be attached to the system board once the signals driven by the system board are defined.

The VmodTFT can only be used with FPGA system boards that support 3.3V supply for the VHDCI connector. For more information, refer to your system board's reference manual at www.digilentinc.com.

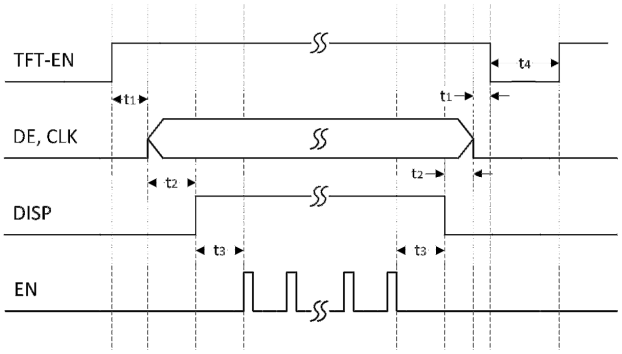


Figure 1 ***Power-Up Sequence***

	Description	Min	Max	Unit
t1	TFT-EN high to first pixel bus signal	0.05	100	ms
t2	Valid pixel data to DISP high	0	200	ms
t3	DISP high to backlight on; backlight off to DISP low	160		ms
t4	TFT-EN low pulse	100		ms

Table 1 ***Power-Up/Reset Timing***

Video Timing

To display an image, the LCD needs to be continuously driven with properly-timed data. This data consists of the lines and blanking periods that form video frames. Each frame consists of 272 active lines and several vertical blanking lines. Each line consists of 480 active pixel periods and several horizontal blanking periods.

Parameter	Description	Value	Unit
fCLK	Pixel clock	9	MHz
tVA	Vertical active period	272	lines
tVB	Vertical blanking period	16	lines
tHA	Horizontal active period	480	CLK periods
tHB	Horizontal blanking period	45	CLK periods

Table 2 ***Typical LCD Video Timing Parameters***

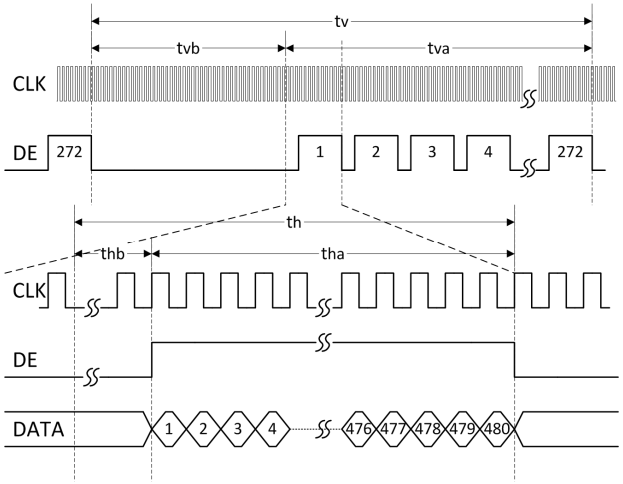


Figure 2 ***Video Timing***

Video data is sent on a parallel interface synchronous to CLK. The table below lists the timing parameters of this interface. “Data” refers to the combined pixel data from the R, G, and B pins.

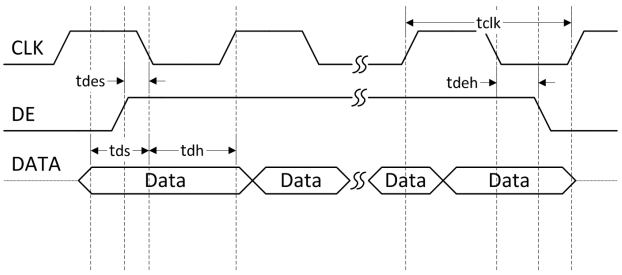


Figure 3 ***AC Characteristics***

	Description	Min	Max	Unit
1/tclk	LCD clock frequency	7	12	MHz
tdes	DE setup before falling CLK	10		ns
tdeh	DE hold before falling CLK	10		ns
tds	Data setup before falling CLK	10		ns
tdh	Data hold before falling CLK	10		ns

Table 3 ***LCD Power-Up/Reset Timing***

Backlight Control

The LED-EN (TFT_BKLT_O) pin provides analog or digital control over the backlight intensity. Jumper JP1 toggles between analog and digital control.

In analog mode, the backlight intensity is set by the voltage divider formed by R7 and R10. Valid values are 0.7V (dimmest) to 1.4V (brightest).

In digital mode, the FPGA can drive this pin with a PWM signal of 100Hz-50kHz.

Touchscreen

The four-wire resistive touchscreen is on top of the LCD. It consists of two conductive transparent layers, one on top of the other, separated by a layer of air. These conductive layers form plates X and Y. Each plate has electrodes on opposite sides and a constant resistance.

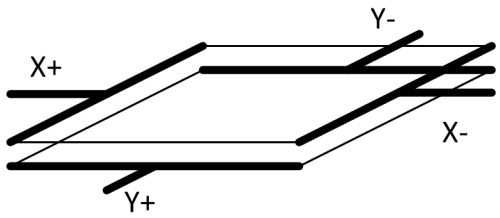


Figure 4 ***Touchscreen Plates X and Y***

When the screen is touched with sufficient force, the two plates make contact and form resistive dividers. By properly biasing the panel and measuring the voltage on the electrodes, the coordinates of the touch can be determined.

For example, tying Y+ and Y- to a power supply, the voltage on either X+ or X- changes linearly to the Y coordinate of the touch. Similarly, supplying power to the X plate and measuring the voltage on the Y electrode determines the X coordinate.

Touch Controller

The VmodTFT uses an AD7873 touch controller to provide an interface for the analog touchscreen to the FPGA. The controller supplies current to the touchscreen and measures the voltage drop using an internal 12-bit analog-to-digital converter. The digitized voltage values are read back by the FPGA so the touch coordinates can be determined.

Theoretically, a digitized voltage drop of 000h (0V) corresponds to a touch very close to the electrode tied to ground. Likewise, a voltage drop of FFFh (VCC) corresponds to a touch very close to the electrode tied to the power supply. However, the actual values measured for the VmodTFT are shown in Table 4.

Touch Corner	X Reading	Y Reading
Top Left	096h	12Ch
Top Right	F6Eh	12Ch
Bottom Left	096h	ED8h
Bottom Right	F6Eh	ED8h

Table 4 **Actual 12-Bit Voltage Readings**

Using these experimental values, the touch coordinates scaled to the LCD active area can be easily determined. Use the following equations, where V_x and V_y are the voltage readings for the X and Y plates.

$$x = \frac{V_x - 96h}{F6Eh - 96h} \times 480$$

$$y = \frac{V_y - 12Ch}{ED8h - 12Ch} \times 272$$

Equation 1 ***Convert Voltage Readings to Coordinates***

Touch can be detected on the PENIRQ interrupt signal. A low value indicates the screen is being touched.

You can also measure the pressure of the touch, referred to as the Z coordinate. The measurement requires a different biasing of the touchscreen and requires some calculation. The equation uses the X and Y plate resistance, which for this panel can be approximated by 1024 and 256 ohms, respectively.

For information on how to use the touch controller to measure touch pressure, refer to the AD7873 datasheet at http://www.analog.com/static/imported-files/data_sheets/AD7873.pdf

VHDCI Connector

The VmodTFT is only compatible with system boards using 3.3V-level signaling and should only be attached to the system board once the signals driven by the system board are defined.

Camera Output	Camera Input

VHDCI	VmodTFT	VHDCI	VmodTFT
IO1-P	TP_BUSY	IO1-N	NC
IO2-P	TP_DIN	IO2-N	TP_DOUT
IO3-P	TP_CS	IO3-N	TP_PENIRQ
IO4-P	TFT_B[5]	IO4-N	TFT_B[7]
IO5-P	TFT_B[4]	IO5-N	TFT_B[6]
IO6-P	TFT_B[2]	IO6-N	TFT_B[3]
IO7-P	TFT_B[0]	IO7-N	TFT_B[1]
IO8-P	TFT_G[6]	IO8-N	TFT_G[7]
IO9-P	TFT_G[5]	IO9-N	TFT_G[4]
IO10-P	TP_DCLK	IO10-N	NC
IO11-P	TFT_CLK	IO11-N	NC
IO12-P	TFT_G[1]	IO12-N	TFT_G[3]
IO13-P	TFT_G[0]	IO13-N	TFT_G[2]
IO14-P	TFT_R[6]	IO14-N	TFT_R[7]
IO15-P	TFT_R[4]	IO15-N	TFT_R[5]
IO16-P	TFT_R[2]	IO16-N	TFT_R[3]
IO17-P	TFT_R[1]	IO17-N	TFT_R[0]
IO18-P	TFT_DISP	IO18-N	TFT_DE
IO19-P	TFT_EN	IO19-N	LED_EN
IO20-P	NC	IO20-N	NC

Table 5 ***VHDCI Connector Pin-Out***

Design Resources

For reference designs, library components and demo projects see www.digilentinc.com.