Xilinx® Virtex™-II Development Kit

by

Avnet Design Services

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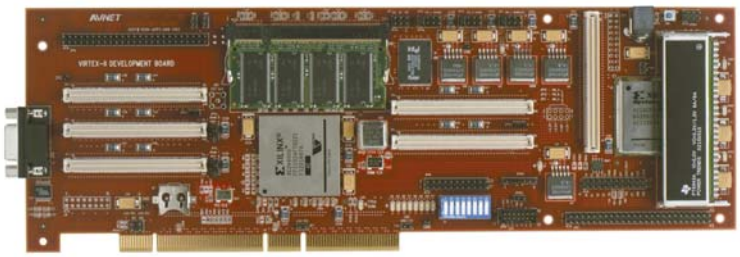
Description

The Virtex-II Development Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the highly advanced Xilinx Virtex-II FPGA family. The installed XC2V1500 device offers a 1.5M system gate prototyping environment to effectively demonstrate the enhanced benefits of the leading edge Xilinx FPGA solution. Embedded multipliers, advanced digital clock management, built-in impedance matching, IP immersion, and other exciting features can be implemented with advanced Xilinx design tools. Demonstration VHDL code is included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

Target Applications:

- High end DSP
- Data transmission and manipulation
- IP based systems
- System connectivity
- High density ASIC replacement



Features

- Xilinx XC2V1500-FF896 Virtex-II FPGA
- Xilinx XCCACEMxx-BG388I System ACE MPM Solution
- 133 MHz, 128 MB DDR SDRAM DIMM powered by Denali Software core
- 16 MB FLASH memory
- +3.3V/+5V, 64-bit 66/100 MHz PCI/PCI-X interface
- Regulated 3.3V, 2.5V, 1.8V and 1.5V supply voltages generated from external 5V supply
- 40MHz, 50MHz, and 125MHz oscillators
- 8 LEDs
- 8 DIP-switches
- Supports Multilynx, Parallel III & Parallel IV JTAG cables
- Connectors for access to FPGA I/O include: 0.1 header connectors and AvBus expansion connectors
- LVDS port
- RS-232 interface

Ordering Information

The following table lists the development system part numbers and available software options. Internet link at http://www.em.avnet.com

Part Number	Hardware
ADS-XLX-V2-DEV1500	Xilinx Virtex-II Development Kit populated with an XC2V1500 device
ADS-XLX-MB-DEV1500	Xilinx Virtex-II Development Kit bundled with Communications/Memory Module and MicroBlaze Core License
ADS-XLX-V2-DEV4000	Xilinx Virtex-II Development Kit populated with an XC2V4000 device
ADS-XLX-MB-DEV4000	Xilinx Virtex-II Development Kit bundled with Communications/Memory Module and MicroBlaze Core License
ADS-XLX-V2-DEV4000XP	Xilinx Virtex-II Development Kit populated with an XC2V4000 device & high-current power supply
ADS-V2-MB-DEV4000XP	Xilinx Virtex-II Development Kit bundled with Communications/Memory Module, MicroBlaze Core License & high-current power supply
ADS-XLX-V2-DEV6000XP	Xilinx Virtex-II Development Kit populated with an XC2V6000 device & high-current power supply
ADS-V2-MB-DEV6000XP	Xilinx Virtex-II Development Kit bundled with Communications/Memory Module, MicroBlaze Core License & high-current power supply

1.0 Introduction and Overview

This document is intended to give the user a basic understanding of the design and use of the Virtex-II Development Board. It will detail the hardware components and their functional purpose.

The Virtex-II Development Kit is part of the Avalon Reference Design System™, provides a baseline development backplane, which incorporates a high density; high I/O Virtex-II FPGA, memory functionality, basic I/O functionality, and interface connections for development module installation. The intent is to provide a functional baseline card development kit with optimal circuit functionality while providing the interface capability to allow the user to add, via the connector interfaces, evaluation boards containing their desired/unique circuit functionality to integrate. The capability to install evaluation boards onto the Virtex-II Development Kit allows FPGA integration between multiple platforms and I/O standards if desired.

The heart of the Virtex-II Development Board is the Xilinx XC2V1500 FPGA, XC2V4000 FPGA or XC2V6000 FPGA. The Virtex-II Field-Programmable Gate Array device utilized in this design is the XC2V1500-5FG896C (528 total I/O) in a FF896 package (fine pitch BGA) or the XC2V4000-4FF1152C or greater (824 total I/O) in a FF1152 package (fine pitch BGA). Configuration information is provided from two sources; the Xilinx Serial/Parallel Download Connectors (JTAG/SelectMAP), or System ACE MPM configuration solution.

The Xilinx FPGA is powered at 3.3V with the core powered at 1.5V. The Virtex-II system block diagram is shown in Figure 1-1.

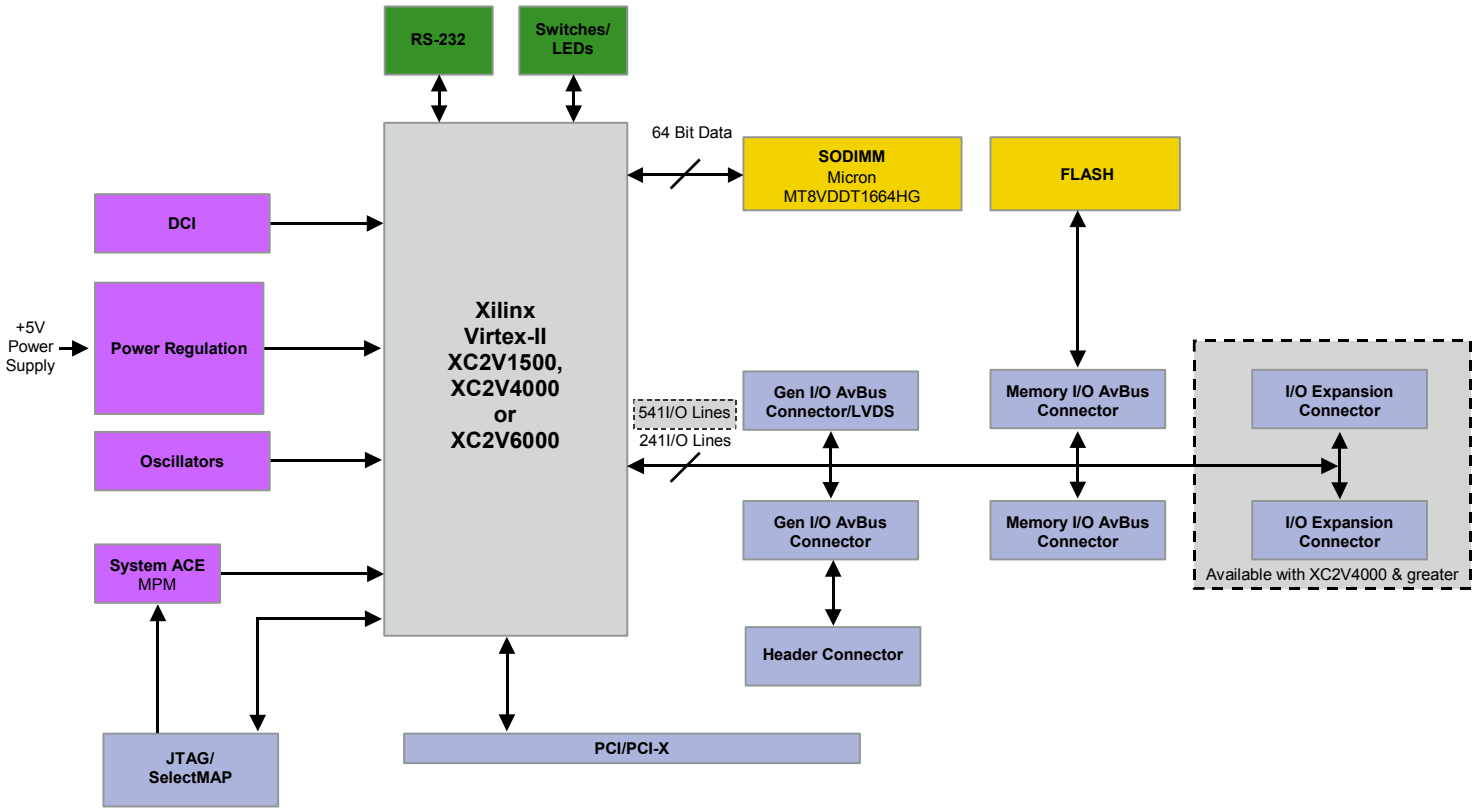


Figure 1-1: System Block Diagram

2.0 Related Documents and Links

The Complete LogiCORE PCI Solution
http://www.xilinx.com/pci/#realpci

LogiCORE PCI-X Virtex-II Interface
http://www.xilinx.com/pci/pci-x.htm

PCI Specification
http://www.pcisig.com

3.0 Hardware Design

The following section details the components found on the Virtex-II Development Board. The Virtex-II Development Board is displayed in Figure 3-1.

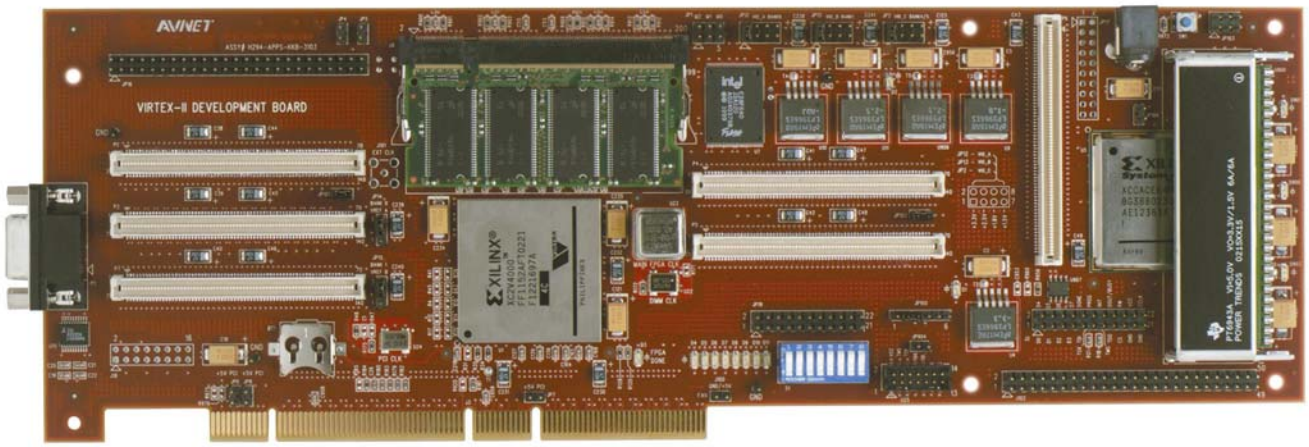


Figure 3-1: Virtex-II Development Board

The chip functionality diagram is shown in Figure 3-2.

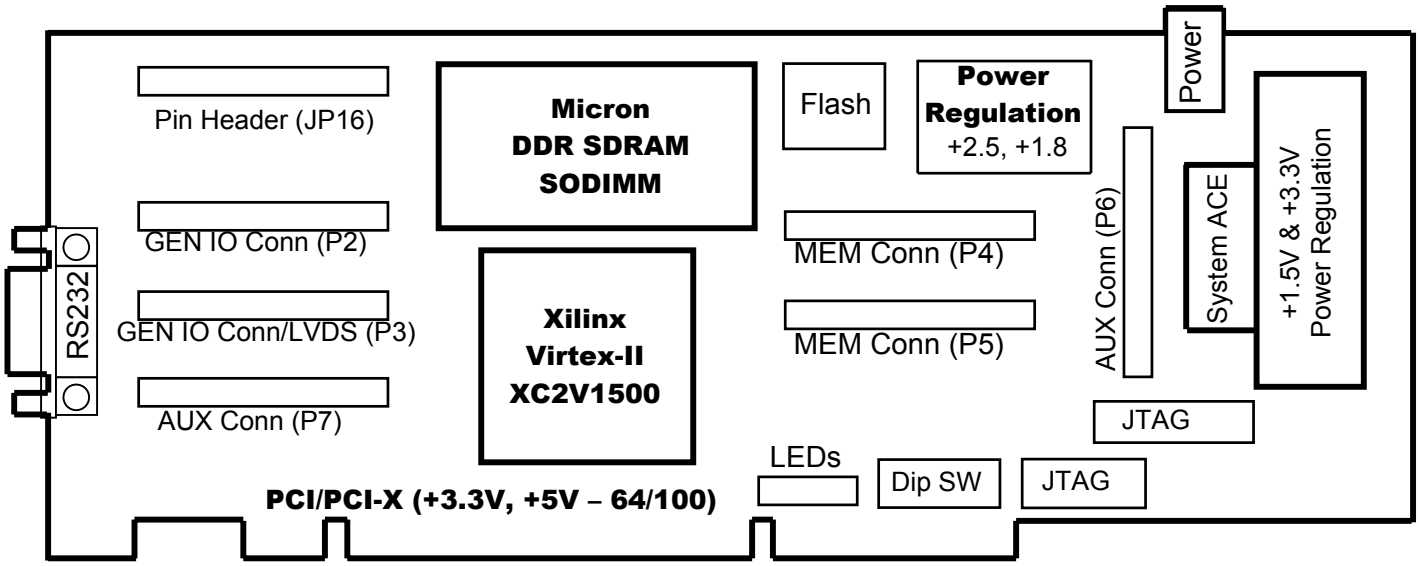


Figure 3-2: Chip Functionality Block - Top Side

3.1 Physical Form Factor

The Virtex-II Development Board Printed Circuit Board (PCB) is a 14-layer board with six signal layers, a +5V power plane incorporating an isolated +1.8V mini plane, 3.3V power plane incorporating an isolated 2.5V & 1.5V mini-plane, and 4 ground planes. A controlled impedance of 50 ohms is used within the PCB to ensure consistent signal integrity. The board stack-up is as follows:

1) Component side / Pads / Signal
2) Power Plane
3) Ground Plane
4) Signal
5) Signal
6) Ground Plane
7) Signal
8) Signal
9) Ground Plane
10) Signal
11) Signal
12) Ground Plane
13) Power Plane
14) Solder Side / Pads / Signal/1.25 mini plane

3.2 Power

The Virtex-II Development Board is powered via the +5.0 volt PCI. However, it may be operated in stand-alone mode. In stand-alone mode the Virtex-II board may be powered by an external power supply connected to the J1 barrel socket connector. The supply should have a minimum of 2 AMP, +5.0 Volts regulated to +/- 5%. The current requirements for the board are application specific. The power connection is shown in Figure 3-3.

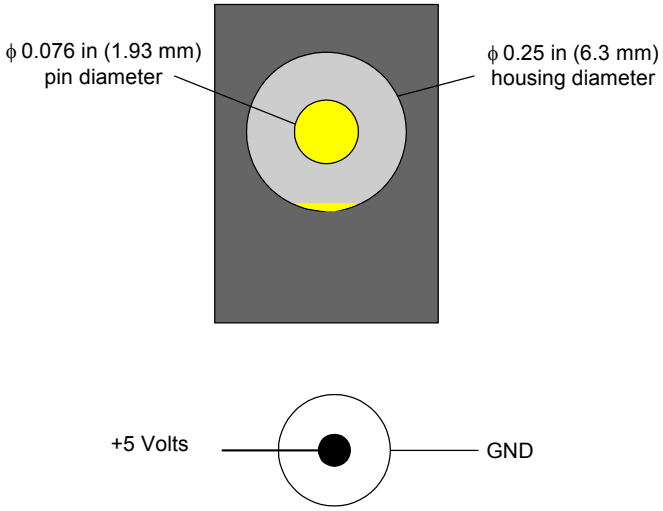


Figure 3-3: External Power Connector J1

The PCI power jumper JP6, 7, 8 configures the board for PCI power mode, jumpers not installed.

3.2.1 FPGA I/O Voltage (Vcco)

Vcco selectable voltages are available on the Virtex-II Development Board to support the FPGAs various voltage standards. The Virtex-II Development Board provides various selectable I/O voltages for FPGA banks 0,1,4 & 5, independent of each other, to support the various I/O standards. The I/O voltages available are +3.3V, +2.5V, +1.8V and +1.5V, these I/O voltage levels are available on header connectors JP12, JP13 & JP2.

3.2.2 FPGA Reference Voltage (Vref)

The Virtex-II Development Board provides various reference voltages for FPGA bank 0 and 1, independent of each other. The reference voltages available are +1.65V, +1.5V, +1.25V, +.9V and +.75V (half the I/O voltage except +1.5V which is jumper selected). These reference voltages are available on header connector JP14 & JP15.

3.3 System ACE MPM Solution

The System ACE Multi-Package Module (MPM) solution addresses the need for a space-efficient, pre-engineered, high-density configuration solution in multiple FPGA systems. A System ACE module (XCCACEMxx-BG388I) has been used in the Virtex-II Development board to support FPGA expandability. As an enhanced, simplified solution and parting from the traditional method of using cascading proms to support FPGA expandability, the system ACE MPM provides all the resources necessary to support the wide range of FPGA expandability of the Virtex-II Development board.

For additional detailed information in using the System ACE with the Virtex-II Development board reference Appendix A.

3.4 Memory

Memory is configured with a 64Bit wide data bus for the DDR SDRAM and 16Bit wide for the FLASH. A common bus is used to connect to the Virtex-II FPGA with the FLASH memory and the memory expansion connector (P4). Chip selects driven by individual Virtex-II pins are utilized to enable/tristate the different memory technologies. In addition, all memory control signals (i.e. FLASH) are assigned to the memory connectors to allow a daughter card evaluation module or processor module access to control the on board memory.

3.4.1 DDR SDRAM

The DDR SDRAM consists of one 128 MB DIMM module (expandable to 512 MB), accessible in a 64-bit configuration and housed in a SODIMM packages. These are LVTTL interface devices running at a maximum 133 MHz (266 Mbits/S). By using the Virtex-II Digital Clock Manager (DCM) the onboard 125.00 MHz frequency can be adjusted to support the DDR SDRAM.

3.4.2 FLASH

The FLASH memory consists of one 16 MB device in a 16-bit configuration. FLASH memories are installed as the default configuration and are powered by 3.3Vdc. The device package is a 56-pin TSOP Type. The current configuration utilizes 25 nanosecond devices, but the Virtex-II FPGA will support much faster devices.

3.5 JTAG

3.5.1 JTAG Chain

The Virtex-II development board has two (2) devices in its JTAG chain (FPGA and System ACE MPM). The JTAG chain is implemented as shown in Figure 3-4. The BSDL files for each device in the chain are given on Table 3-1.

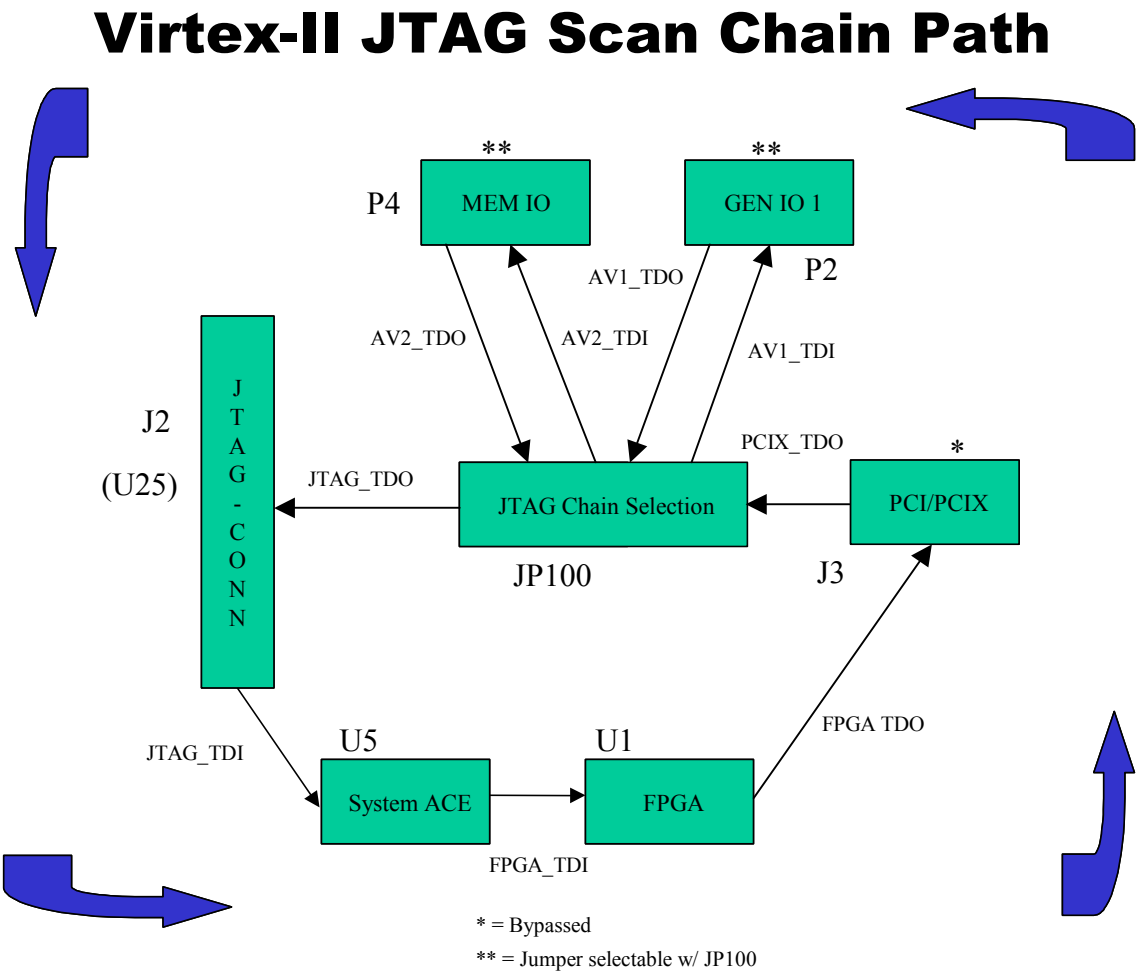


Figure 3-4: JTAG Chain

File Name	Device	Device Reference Designator
XC2V1500_FF896.bsd	FPGA	U1
XC2V4000_FF1152.bsd	FPGA	U1
XCCACEMxx_BG388.bsd	SYSTEM ACE	U5

Table 3-1: JTAG Boundary-Scan Description Language (BSDL) files

3.5.2 JTAG/SelectMAP Header

The JTAG Header (J2) provides both the JTAG and SelectMAP inputs for the FPGA and System ACE MPM. In addition, a second JTAG header (U25) has been provided to support the Xilinx Parallel IV cable. Inputs on the JTAG header are described in Table 3-2.

Signal Name	Download Connector Pin #
D0 / Din	1
D1	2
D2	3
D3	4
D4	5
D5	6
D6	7
D7	8
TDI	9 (U25-10)
DONE	10
TCK	11 (U25-6)
PROG	12
TMS	13 (U25-4)
INIT	14
TDO	15 (U25-8)
Dout / BUSY	16
CS	17
R/W	18
GND	19
VCC	20
GND	21
CCLK	22

Table 3-2: JTAG/SelectMAP Header Connector (J2 & U25) Pin Assignment

Note: Use impact version 4.2i service pack 3 or any upgraded version for programming System ACE MPM. Please see read-me file on CD in the System ACE folder for latest related instructions.

3.6 LED

The "DONE" LED (D3) is driven from the PROG_DONE pin on the FPGA. The output is pulled low in hardware causing the LED to be 'on' when the FPGA has completed program end.

8 LED's are provided for testing purposes. The pin assignment for the LEDs is provided in Table 3-3.

LED	1500 Pin	4000 Pin	Pin Description
LED0	L7	N9	LED0
LED1	M6	P8	LED1
LED2	L6	N8	LED2
LED3	L5	N7	LED3
LED4	K4	M6	LED4
LED5	K1	M3	LED5
LED6	J4	L6	LED6
LED7	J1	L3	LED7

Table 3-3: LED Pin Assignment @ the FPGA

3.7 DIP Switches

An 8-position DIP-switch is mounted on the board and labeled "S1".

The Virtex-II Development Board is shipped with basic demonstration code (exercise UART & FLASH) loaded in the System ACE MPM solution. This demonstration code is used to show functionality of the board. Upon power-up, in Master-Serial mode (see Table 3-11), the FPGA will be programmed from the System ACE MPM.

Sample code is provided to exercise the UART & LED scanning.

1. S1-1, when ON, will enable the LEDs to start scanning.
2. S1-1, when OFF, and S1-2 ON and S1-3 ON will enable the UART. Upon enabling the UART the following message will be displayed:

AVNET DESIGN SERVICES
design@ads.avnet.com
1.800.585.1602
www.ads.avnet.com
Virtex-II Development Board

See Figure 3-5 DIP-switch operation for switch positions and Table 3-4 for switch pin assignments at the FPGA.

Note:
Communication to the UART can be accomplished with Hyper Terminal. To establish communication correctly Configure Hyper Terminal as follows:

Name	Configuration Value
Baud Rate	19,200 (demo code) 9600 (sample code)
Data bits	8
Stop bit	1
Parity	None
Flow Control	None

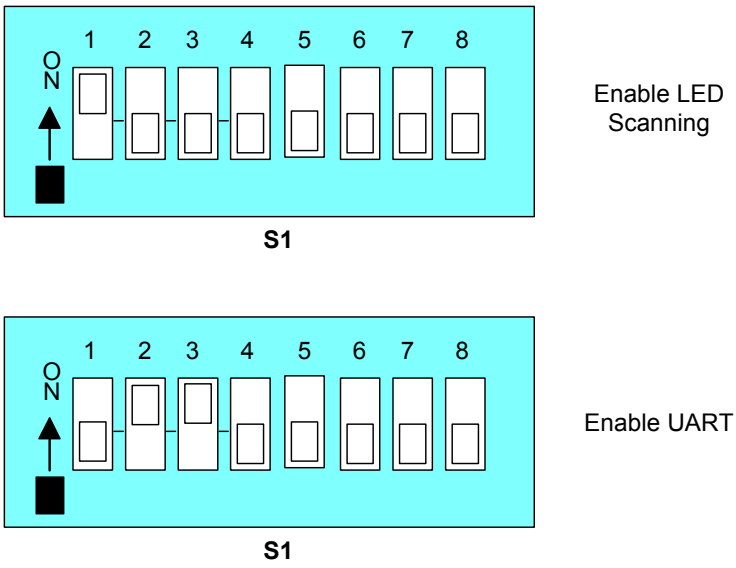


Figure 3-5: DIP-Switch Operation

SWITCH	1500 Pin	4000 Pin	Pin Description
SWITCH0	AJ1	AL3	SWITCH0
SWITCH1	AH1	AK3	SWITCH1
SWITCH2	AG3	AJ5	SWITCH2
SWITCH3	AF4	AH6	SWITCH3
SWITCH4	AE5	AG7	SWITCH4
SWITCH5	AD5	AF7	SWITCH5
SWITCH6	AD9	AF11	SWITCH6
SWITCH7	AC9	AE11	SWITCH7

Table 3-4: Switch Pin Assignment @ the FPGA

3.8 ASYNCHRONOUS (RS-232) COMMUNICATION INTERFACE

The ADM3222 is a high-speed, 2-channel RS-232/V.28 interface device that operates from a single +3.3 V power supply. A single port is utilized to interface with the FPGA. Low power consumption and a shutdown facility are among some of the component highlights. The ADM3222 conforms to the EIA-232E and CCITT V.28 specifications and operate at data rates up to 230 kbps. The AM3222 contains additional enable and shutdown circuitry. See Table 3-5 for RS-232 connector pin assignment.

The ADM3222 is packaged in a SO20.

Signal Name	DB9 Connector Def.
TX out	2
RX in	3
GND	5

Table 3-5: RS-232 Connector Pin Assignment – P1

3.9 CONNECTORS

General I/O, memory expansion, and auxiliary connector interface are provided for user flexibility. The general I/O, memory expansion, and auxiliary (available only with FF1152 package) connectors are predefined with a common pin-out definition to provide a high-speed signal quality solution. This pin-out standard has been designated as the AvBus connector standard. It is comprised of a 2:1 signal to power/ground ratio, which is implemented to ensure signal integrity, and controlled impedance continuity. The connectors used are AMP 140 pin; .8mm connectors part no. 179031-6, which realize an effective I/O count of 241 signals with the X2V1500 part or 541 signals with the X2V4000 or greater part.

Various mating height definitions 177983-6, 5-179009-6 & 5-179010-6 (8 mm, 12 mm & 16 mm) can be implemented to accommodate any mechanical interface constraints with the installation of the evaluation modules.

Note: Signals shown in color RED are only available with large FPGA package FF1152.

3.9.1 GENERAL I/O INTERFACE

A general I/O interface allows the user to adapt any desired functionality to the development kit backplane for research and development. The FPGA connections to these connectors utilizes a high I/O interface, thus allowing the user to select the installation requirements for the development module. Two 140-pin connectors are paired to provide this interface. See Table 3-6 for general I/O AvBus connector pin assignment. Signal routing from the FPGA to connector P3 is routed as LVDS pairs, allowing connector P3 to supports LVDS signaling.

Name	P2 Connector Pin #			Name	Name	P3 Connector Pin #			Name
GEN_IO1_0	71		1	+5V	GEN_IO2_0	71		1	+5V
GND	72		2	GEN_IO1_1	GND	72		2	GEN_IO2_1
GEN_IO1_3	73		3	GEN_IO1_2	GEN_IO2_3	73		3	GEN_IO2_2
GEN_IO1_4	74		4	GND	GEN_IO2_4	74		4	GND
GND	75		5	GEN_IO1_5	GND	75		5	GEN_IO2_5
GEN_IO1_7	76		6	GEN_IO1_6	GEN_IO2_7	76		6	GEN_IO2_6
GEN_IO1_8	77		7	GND	GEN_IO2_8	77		7	GND
+3.3V	78		8	GEN_IO1_9	+3.3V	78		8	GEN_IO2_9
GEN_IO1_11	79		9	GEN_IO1_10	GEN_IO2_11	79		9	GEN_IO2_10
GEN_IO1_12	80		10	GND	GEN_IO2_12	80		10	GND
GND	81		11	GEN_IO1_13	GND	81		11	GEN_IO2_13
GEN_IO1_15	82		12	GEN_IO1_14	GEN_IO2_15	82		12	GEN_IO2_14

P2 Name	P2 Connector Pin #			P2 Name	P3 Name	P3 Connector Pin #			P3 Name
GEN_IO1_16	83		13	+5V	GEN_IO2_16	83		13	+5V
GND	84		14	GEN_IO1_17	GND	84		14	GEN_IO2_17
GEN_IO1_19	85		15	GEN_IO1_18	GEN_IO2_19	85		15	GEN_IO2_18
GEN_IO1_20	86		16	GND	GEN_IO2_20	86		16	GND
GND	87		17	GEN_IO1_21	GND	87		17	GEN_IO2_21
GEN_IO1_23	88		18	GEN_IO1_22	GEN_IO2_23	88		18	GEN_IO2_22
GEN_IO1_24	89		19	GND	GEN_IO2_24	89		19	GND
+3.3V	90		20	GEN_IO1_25	+3.3V	90		20	GEN_IO2_25
GEN_IO1_27	91		21	GEN_IO1_26	GEN_IO2_27	91		21	GEN_IO2_26
GEN_IO1_28	92		22	GND	GEN_IO2_28	92		22	GND
GND	93		23	GEN_IO1_29	GND	93		23	GEN_IO2_29
GEN_IO1_31	94		24	GEN_IO1_30	GEN_IO2_31	94		24	GEN_IO2_30
GEN_IO1_32	95		25	+5V	GEN_IO2_32	95		25	+5V
GND	96		26	GEN_IO1_33	GND	96		26	GEN_IO2_33
GEN_IO1_35	97		27	GEN_IO1_34	GEN_IO2_35	97		27	GEN_IO2_34
GEN_IO1_36	98		28	GND	GEN_IO2_36	98		28	GND
GND	99		29	GEN_IO1_37	GND	99		29	GEN_IO2_37
GEN_IO1_39	100		30	GEN_IO1_38	GEN_IO2_39	100		30	GEN_IO2_38
GEN_IO1_40	101		31	GND	GEN_IO2_40	101		31	GND
+3.3V	102		32	GEN_IO1_41	+3.3V	102		32	GEN_IO2_41
GEN_IO1_43	103		33	GEN_IO1_42	GEN_IO2_43	103		33	GEN_IO2_42
GEN_IO1_44	104		34	GND	GEN_IO2_44	104		34	GND
GND	105		35	GEN_IO1_45	GND	105		35	GEN_IO2_45
GEN_IO1_47	106		36	GEN_IO1_46	GEN_IO2_47	106		36	GEN_IO2_46
GEN_IO1_48	107		37	+5V	GEN_IO2_48	107		37	+5V
GND	108		38	GEN_IO1_49	GND	108		38	GEN_IO2_49
GEN_IO1_51	109		39	GEN_IO1_50	GEN_IO2_51	109		39	GEN_IO2_50
GEN_IO1_52	110		40	GND	GEN_IO2_52	110		40	GND
GND	111		41	GEN_IO1_53	GND	111		41	GEN_IO2_53
GEN_IO1_55	112		42	GEN_IO1_54	GEN_IO2_55	112		42	GEN_IO2_54
GEN_IO1_56	113		43	GND	GEN_IO2_56	113		43	GND
+3.3V	114		44	GEN_IO1_57	+3.3V	114		44	GEN_IO2_57
GEN_IO1_59	115		45	GEN_IO1_58	GEN_IO2_59	115		45	GEN_IO2_58
GEN_IO1_60	116		46	GND	GEN_IO2_60	116		46	GND
GND	117		47	GEN_IO1_61	GND	117		47	GEN_IO2_61
GEN_IO1_63	118		48	GEN_IO1_62	GEN_IO2_63	118		48	GEN_IO2_62
GEN_IO1_64	119		49	+5V	GEN_IO2_64	119		49	+5V
GND	120		50	GEN_IO1_65	GND	120		50	GEN_IO2_65
GEN_IO1_67	121		51	GEN_IO1_66	GEN_IO2_67	121		51	GEN_IO2_66
GEN_IO1_68	122		52	GND	GEN_IO2_68	122		52	GND
GND	123		53	GEN_IO1_69	GND	123		53	GEN_IO2_69
GEN_IO1_71	124		54	GEN_IO1_70	GEN_IO2_71	124		54	GEN_IO2_70
GEN_IO1_72	125		55	GND	GEN_IO2_72	125		55	GND
+3.3V	126		56	GEN_IO1_73	+3.3V	126		56	GEN_IO2_73
GEN_IO1_75	127		57	GEN_IO1_74	GEN_IO2_75	127		57	GEN_IO2_74
GEN_IO1_76	128		58	GND	GEN_IO2_76	128		58	GND
GND	129		59	GEN_IO1_77	GND	129		59	GEN_IO2_77
GEN_IO1_79	130		60	GEN_IO1_78	GEN_IO2_79	130		60	GEN_IO2_78
GEN_IO1_80	131		61	+5V	GEN_IO2_80	131		61	+5V
GND	132		62	GEN_IO1_81	GND	132		62	GEN_IO2_81
GEN_IO1_83	133		63	GEN_IO1_82	GEN_IO2_83	133		63	GEN_IO2_82
GEN_IO1_84	134		64	GND	GEN_IO2_84	134		64	GND
GND	135		65	GEN_IO1_CLK_OUT	GND	135		65	
GEN_IO1_CLKIN	136		66	GEN_IO1_CLK_FB	GEN_IO2_CLK IN	136		66	
TMS	137		67	GND		137		67	GND
+3.3V	138		68	AV1_TDO	+3.3V	138		68	GEN_IO1_CLK_OUT

Name	P2 Connector Pin #			Name		Name	P3 Connector Pin #			Name
AV1_TDI	139		69	TCK			139		69	GEN_IO1_CLK_FB
TRST#	140		70	GND			140		70	GND

Table 3-6: General I/O AvBus Connector P2 & P3

3.9.1.1 LVDS

Low Voltage Differential Signaling (LVDS) is available on connector P3. Eleven LVDS driver pairs and eleven LVDS receiver pairs (optional drivers) are available. An additional thirteen LVDS driver pairs (two of which are optional receivers) are available with a larger FPGA package – FF1152. See Table 3-7.

Name	P3 Connector Drivers			Name		Name	P3 Connector Receivers			Name
GEN_IO2_3	1		15	GEN_IO2_57		GEN_IO2_1	* 1			
GEN_IO2_4				GEN_IO2_58		GEN_IO2_2				
GEN_IO2_7	2		* 16	GEN_IO2_59		GEN_IO2_5	* 2			
GEN_IO2_8				GEN_IO2_60		GEN_IO2_6				
GEN_IO2_11	3		17	GEN_IO2_61		GEN_IO2_9	* 3			
GEN_IO2_12				GEN_IO2_62		GEN_IO2_10				
GEN_IO2_15	4		* 18	GEN_IO2_63		GEN_IO2_13	* 4			
GEN_IO2_16				GEN_IO2_64		GEN_IO2_14				
GEN_IO2_19	5		* 19	GEN_IO2_65		GEN_IO2_17	* 5			
GEN_IO2_20				GEN_IO2_66		GEN_IO2_18				
GEN_IO2_23	6		* 20	GEN_IO2_67		GEN_IO2_21	* 6			
GEN_IO2_24				GEN_IO2_68		GEN_IO2_22				
GEN_IO2_27	7		* 21	GEN_IO2_69		GEN_IO2_25	* 7			
GEN_IO2_28				GEN_IO2_70		GEN_IO2_26				
GEN_IO2_31	8		* 22	GEN_IO2_71		GEN_IO2_29	* 8			
GEN_IO2_32				GEN_IO2_72		GEN_IO2_30				
GEN_IO2_35	9		* 23	GEN_IO2_73		GEN_IO2_33	* 9			
GEN_IO2_36				GEN_IO2_74		GEN_IO2_34				
GEN_IO2_39	10		* 24	GEN_IO2_75		GEN_IO2_37	* 10			
GEN_IO2_40				GEN_IO2_76		GEN_IO2_38				
GEN_IO2_43	11		* 25	GEN_IO2_77		GEN_IO2_41	* 11			
GEN_IO2_44				GEN_IO2_78		GEN_IO2_42				
GEN_IO2_51	12		* 26	GEN_IO2_79						
GEN_IO2_52				GEN_IO2_80						
GEN_IO2_53	13		* 27	GEN_IO2_81						
GEN_IO2_54				GEN_IO2_82						
GEN_IO2_55	14									
GEN_IO2_56										

* = Optional Driver/Receiver

Table 3-7: Low Voltage Differential Signaling Pairs (P3)

3.9.2 MEMORY EXPANSION CONNECTOR INTERFACE

A memory expansion interface interconnects the memory signals to the development module for the option to implement increased memory capabilities, different memory technologies or a host controller. In addition to the standard memory signals, additional spare I/O signals are routed to the connector to allow for arbitration and control. Unknown bus loading from the development module must be considered to ensure the local memory bus functionality with all types of development modules installed. Two 140-pin connectors are paired to provide this interface. See Table 3-8 for memory AvBus connector pin assignment.

Name	P4 Connector Pin #		Name	Name	P5 Connector Pin #		Name
ADDR_AV0	71	1	+5V	DATA_AV32	71	1	+5V
GND	72	2	ADDR_AV1	GND	72	2	DATA_AV33
ADDR_AV3	73	3	ADDR_AV2	DATA_AV35	73	3	DATA_AV34
ADDR_AV4	74	4	GND	DATA_AV36	74	4	GND
GND	75	5	ADDR_AV5	GND	75	5	DATA_AV37
ADDR_AV7	76	6	ADDR_AV6	DATA_AV39	76	6	DATA_AV38
ADDR_AV8	77	7	GND	DATA_AV40	77	7	GND
+3.3V	78	8	ADDR_AV9	+3.3V	78	8	DATA_AV41
ADDR_AV11	79	9	ADDR_AV10	DATA_AV43	79	9	DATA_AV42
ADDR_AV12	80	10	GND	DATA_AV44	80	10	GND
GND	81	11	ADDR_AV13	GND	81	11	DATA_AV45
ADDR_AV15	82	12	ADDR_AV14	DATA_AV47	82	12	DATA_AV46
ADDR_AV16	83	13	+5V	DATA_AV48	83	13	+5V
GND	84	14	ADDR_AV17	GND	84	14	DATA_AV49
ADDR_AV19	85	15	ADDR_AV18	DATA_AV51	85	15	DATA_AV50
ADDR_AV20	86	16	GND	DATA_AV52	86	16	GND
GND	87	17	ADDR_AV21	GND	87	17	DATA_AV53
ADDR_AV23	88	18	ADDR_AV22	DATA_AV55	88	18	DATA_AV54
ADDR_AV24	89	19	GND	DATA_AV56	89	19	GND
+3.3V	90	20	ADDR_AV25	+3.3V	90	20	DATA_AV57
ADDR_AV27	91	21	ADDR_AV26	DATA_AV59	91	21	DATA_AV58
ADDR_AV28	92	22	GND	DATA_AV60	92	22	GND
GND	93	23	ADDR_AV29	GND	93	23	DATA_AV61
ADDR_AV31	94	24	ADDR_AV30	DATA_AV63	94	24	DATA_AV62
DATA_AV0	95	25	+5V	FLASH_CE2#	95	25	+5V
GND	96	26	DATA_AV1	GND	96	26	FLASH_CE3#
DATA_AV3	97	27	DATA_AV2	SDRAM_BYTE5	97	27	SDRAM_BYTE4
DATA_AV4	98	28	GND	SDRAM_BYTE6	98	28	GND
GND	99	29	DATA_AV5	GND	99	29	SDRAM_BYTE7
DATA_AV7	100	30	DATA_AV6	MEM_IO_7	100	30	MEM_IO_6
DATA_AV8	101	31	GND	MEM_IO_8	101	31	GND
+3.3V	102	32	DATA_AV9	+3.3V	102	32	MEM_IO_9
DATA_AV11	103	33	DATA_AV10	MEM_IO_11	103	33	MEM_IO_10
DATA_AV12	104	34	GND	MEM_IO_12	104	34	GND
GND	105	35	DATA_AV13	GND	105	35	MEM_IO_13
DATA_AV15	106	36	DATA_AV14	MEM_IO_15	106	36	MEM_IO_14
DATA_AV16	107	37	+5V	MEM_IO_16	107	37	+5V
GND	108	38	DATA_AV17	GND	108	38	MEM_IO_17

Name	P4 Connector Pin #		Name	Name	P5 Connector Pin #		Name
DATA_AV19	109	39	DATA_AV18	MEM_IO_19	109	39	MEM_IO_18
DATA_AV20	110	40	GND	MEM_IO_20	110	40	GND
GND	111	41	DATA_AV21	GND	111	41	MEM_IO_21
DATA_AV23	112	42	DATA_AV22	MEM_IO_23	112	42	MEM_IO_22
DATA_AV24	113	43	GND	MEM_IO_24	113	43	GND
+3.3V	114	44	DATA_AV25	+3.3V	114	44	MEM_IO_25
DATA_AV27	115	45	DATA_AV26	MEM_IO_27	115	45	MEM_IO_26
DATA_AV28	116	46	GND	MEM_IO_28	116	46	GND
GND	117	47	DATA_AV29	GND	117	47	MEM_IO_29
DATA_AV31	118	48	DATA_AV30	MEM_IO_31	118	48	MEM_IO_30
FLASH_CE0#	119	49	+5V	MEM_IO_32	119	49	+5V
GND	120	50	FLASH_CE1#	GND	120	50	MEM_IO_33
FLASH_WE#	121	51	FLASH_OE#	MEM_IO_35	121	51	MEM_IO_34
FLASH_RST#	122	52	GND	MEM_IO_36	122	52	GND
GND	123	53	SDRAM_CS#	+3.3V	123	53	MEM_IO_37
SDRAM_WE#	124	54	SDRAM_CAS#	MEM_IO_39	124	54	MEM_IO_38
SDRAM_CLK	125	55	GND	MEM_IO_40	125	55	GND
+3.3V	126	56	SDRAM_RAS#	GND	126	56	MEM_IO_41
SDRAM_BYTE0	127	57	SDRAM_CLKEN	MEM_IO_43	127	57	MEM_IO_42
SDRAM_BYTE1	128	58	GND	MEM_IO_44	128	58	+5V
GND	129	59	SDRAM_BYTE2	GND	129	59	MEM_IO_45
MEM_IO_0	130	60	SDRAM_BYTE3	MEM_IO_47	130	60	MEM_IO_46
MEM_IO_1	131	61	+5V	MEM_IO_48	131	61	GND
GND	132	62	MEM_IO_2	GND	132	62	MEM_IO_49
MEM_IO_4	133	63	MEM_IO_3	MEM_IO_51	133	63	MEM_IO_50
MEM_IO_5	134	64	GND	MEM_IO_52	134	64	GND
GND	135	65	MEM_IO_CLKOUT	+3.3V	135	65	MEM_IO_53
MEM_IO_CLKIN	136	66	MEM_IO_CLK_FB	MEM_IO_55	136	66	MEM_IO_54
TMS	137	67	GND	MEM_IO_56	137	67	GND
+3.3V	138	68	AV2_TDO	GND	138	68	MEM_IO_57
AV2_TDI	139	69	TCK	MEM_IO_59	139	69	MEM_IO_58
TRST#	140	70	GND	MEM_IO_60	140	70	GND

Table 3-8: Memory I/O AvBus Connector P4 & P5

3.9.3 AUXILIARY CONNECTORS (Available only with FF1152 package)

The additional auxilary I/O interface allows the user to adapt any desired functionality to the development kit backplane for research and development. Connector P6 is configured for a I/O voltage (VCCO) of 2.5V and connector P7 for a I/O voltage (VCCO) of 3.3V. The FPGA connections to these connectors utilizes a high I/O interface, thus allowing the user to select the installation requirements for the development module. Two 140-pin connectors are paired to provide this interface. See Table 3-9 for general I/O AvBus connector pin assignment.

Name	P6 Connector Pin #		Name	Name	P7 Connector Pin #		Name
V25_IO_0	71	1	+5V	V33_IO_0	71	1	+5V
GND	72	2	V25_IO_1	GND	72	2	V33_IO_1
V25_IO_3	73	3	V25_IO_2	V33_IO_3	73	3	V33_IO_2
V25_IO_4	74	4	GND	V33_IO_4	74	4	GND
GND	75	5	V25_IO_5	GND	75	5	V33_IO_5

P6 Name	P6 Connector Pin #		P6 Connector Pin #	P6 Name	P7 Name	P7 Connector Pin #		P7 Connector Pin #	P7 Name
V25_IO_7	76		6	V25_IO_6	V33_IO_7	76		6	V33_IO_6
V25_IO_8	77		7	GND	V33_IO_8	77		7	GND
+3.3V	78		8	V25_IO_9	+3.3V	78		8	V33_IO_9
V25_IO_11	79		9	V25_IO_10	V33_IO_11	79		9	V33_IO_10
V25_IO_12	80		10	GND	V33_IO_12	80		10	GND
GND	81		11	V25_IO_13	GND	81		11	V33_IO_13
V25_IO_15	82		12	V25_IO_14	V33_IO_15	82		12	V33_IO_14
V25_IO_16	83		13	+5V	V33_IO_16	83		13	+5V
GND	84		14	V25_IO_17	GND	84		14	V33_IO_17
V25_IO_19	85		15	V25_IO_18	V33_IO_19	85		15	V33_IO_18
V25_IO_20	86		16	GND	V33_IO_20	86		16	GND
GND	87		17	V25_IO_21	GND	87		17	V33_IO_21
V25_IO_23	88		18	V25_IO_22	V33_IO_23	88		18	V33_IO_22
V25_IO_24	89		19	GND	V33_IO_24	89		19	GND
+3.3V	90		20	V25_IO_25	+3.3V	90		20	V33_IO_25
V25_IO_27	91		21	V25_IO_26	V33_IO_27	91		21	V33_IO_26
V25_IO_28	92		22	GND	V33_IO_28	92		22	GND
GND	93		23	V25_IO_29	GND	93		23	V33_IO_29
V25_IO_31	94		24	V25_IO_30	V33_IO_31	94		24	V33_IO_30
V25_IO_32	95		25	+5V	V33_IO_32	95		25	+5V
GND	96		26	V25_IO_33	GND	96		26	V33_IO_33
V25_IO_35	97		27	V25_IO_34	V33_IO_35	97		27	V33_IO_34
V25_IO_36	98		28	GND	V33_IO_36	98		28	GND
GND	99		29	V25_IO_37	GND	99		29	V33_IO_37
V25_IO_39	100		30	V25_IO_38	V33_IO_39	100		30	V33_IO_38
V25_IO_40	101		31	GND	V33_IO_40	101		31	GND
+3.3V	102		32	V25_IO_41	+3.3V	102		32	V33_IO_41
V25_IO_43	103		33	V25_IO_42	V33_IO_43	103		33	V33_IO_42
V25_IO_44	104		34	GND	V33_IO_44	104		34	GND
GND	105		35	V25_IO_45	GND	105		35	V33_IO_45
V25_IO_47	106		36	V25_IO_46	V33_IO_47	106		36	V33_IO_46
V25_IO_48	107		37	+5V	V33_IO_48	107		37	+5V
GND	108		38	V25_IO_49	GND	108		38	V33_IO_49
V25_IO_51	109		39	V25_IO_50	V33_IO_51	109		39	V33_IO_50
V25_IO_52	110		40	GND	V33_IO_52	110		40	GND
GND	111		41	V25_IO_53	GND	111		41	V33_IO_53
V25_IO_55	112		42	V25_IO_54	V33_IO_55	112		42	V33_IO_54
V25_IO_56	113		43	GND	V33_IO_56	113		43	GND
+3.3V	114		44	V25_IO_57	+3.3V	114		44	V33_IO_57
V25_IO_59	115		45	V25_IO_58	V33_IO_59	115		45	V33_IO_58
V25_IO_60	116		46	GND	V33_IO_60	116		46	GND
GND	117		47	V25_IO_61	GND	117		47	V33_IO_61
V25_IO_63	118		48	V25_IO_62	V33_IO_63	118		48	V33_IO_62
V25_IO_64	119		49	+5V	V33_IO_64	119		49	+5V
GND	120		50	V25_IO_65	GND	120		50	V33_IO_65
V25_IO_67	121		51	V25_IO_66	V33_IO_67	121		51	V33_IO_66
V25_IO_68	122		52	GND	V33_IO_68	122		52	GND
GND	123		53	V25_IO_69	GND	123		53	V33_IO_69
V25_IO_71	124		54	V25_IO_70	V33_IO_71	124		54	V33_IO_70
V25_IO_72	125		55	GND	V33_IO_72	125		55	GND
+3.3V	126		56	V25_IO_73	+3.3V	126		56	V33_IO_73
V25_IO_75	127		57	V25_IO_74	V33_IO_75	127		57	V33_IO_74
V25_IO_76	128		58	GND	V33_IO_76	128		58	GND
GND	129		59	V25_IO_77	GND	129		59	V33_IO_77
V25_IO_79	130		60	V25_IO_78	V33_IO_79	130		60	V33_IO_78
V25_IO_80	131		61	+5V	V33_IO_80	131		61	+5V
GND	132		62	V25_IO_81	GND	132		62	V33_IO_81

P6 Name	P6 Connector Pin #			P6 Name	P7 Name	P7 Connector Pin #			P7 Name
V25_IO_83	133		63	V25_IO_82	V33_IO_83	133		63	V33_IO_82
V25_IO_84	134		64	GND	V33_IO_84	134		64	GND
GND	135		65		GND	135		65	V33_IO_85
	136		66		LED0	136		66	V33_IO_86
	137		67	GND	LED1	137		67	GND
+3.3V	138		68		+3.3V	138		68	LED2
	139		69		LED4	139		69	LED3
	140		70	GND	LED5	140		70	GND
					GND				

Table 3-9: Auxiliary AvBus Connector P6 & P7

3.9.4 MISCELLANEOUS CONNECTORS

- Various support connectors are installed for I/O, power, and programming for the backplane.
- I/O connectors include RS-232e.
- Power connectors include a +5V barrel type connector for sourcing the power regulators and on board circuitry.
- High-density Mictor connectors are provided which allow accessibility to the signals between the FPGA and the I/O resources on the board. These connectors allow the user to monitor signal flow during the development process for the FPGA cores.
- For programming the FPGA, a Xilinx parallel/serial connector (Parallel III & MultiLINX) and a JTAG connector (Parallel IV) are provided.

3.10 PCI/PCI-X

The Virtex-II board PCI/PCI-X interfaces to a PCI bus and hence the outside world. The Virtex-II FPGA is connected to the PCI/PCI-X bus and provides control functions provided that the Xilinx PCI-X LogiCORE is implemented. (Xilinx PCI-X LogiCORE not included).

The PCI-X bus interface is designed as a +3.3V/+5V, 64-Bit, 66/100MHz interface compatible with PCI/PCI-X per standard PCI LOCAL BUS SPECIFICATION Revision 2.1S. A standard PCI connector is implemented to provide a card connection to PC platform. The Virtex-II™ device is placed as close as possible to the PCI

connectors to facilitate clock/signal routing consistent with the requirements imposed by the PCI 2.1S. All PCI functionality is provided by Virtex-II firmware. ±12V power available from the PCI bus is not used.

If the PCI/PCI-X interface is not required, this board may be plugged into a mating receptacle and the 87 dedicated Virtex-II I/O lines may be used for other applications. The bus is intended to provide adequate bandwidth for a customer to implement a usable PCI/PCI-X interface at the Virtex-II data rates. It is intended, for example, to be an integral interface to a high-end workstation as part of the final product. That is, the final product implements 64 bit PCI/PCI-X. It is not intended as a low bandwidth control port to allow designers the convenience of placing the board in a PC at their desk for emulation. If the end application is a +3.3V OR +5V, 64/66/100 PCI/PCI-X, then the customer will likely have a suitable test bed available. See Table 3-10 for the PCI Connector Pin assignment.

PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #
-12V	B1		GND	B34		C/BE[6]#	B65
TRST#	A1		FRAME#	A34		C/BE[5]#	A65
TCK	B2		IRDY#	B35		C/BE[4]#	B66
+12V	A2		GND	A35		n/c	A66
GND	B3		+3.3V	B36		GND	B67
TMS	A3		TRDY# @	A36		PAR64	A67
TDO	B4		DEVSEL# @	B37		AD[63]	B68
TDI	A4		GND	A37		AD[62]	A68
+5V	B5		PCIXCAP	B38		AD[61	B69
+5V	A5		STOP# @	A38		GND	A69
+5V	B6		LOCK	B39		n/c	B70
INTA#	A6		+3.3V	A39		AD[60]	A70
INTB#	B7		PERR# @	B40		AD[59]	B71
INTC#	A7		SDONE	A40		AD[58]	A71
INTD#	B8		+3.3V	B41		AD[57]	B72
+5V	A8		SBO#	A41		GND	A72
PRSNT1#	B9		SERR#	B42		GND	B73
n/c	A9		GND	A42		AD[56]	A73
n/c	B10		+3.3V	B43		AD[55]	B74
n/c	A10		PAR	A43		AD[54]	A74
PRSNT2#	B11		C/BE[1]#	B44		AD[53]	B75
n/c	A11		AD[15]	A44		n/c	A75
n/c	B14		AD[14]	B45		GND	B76
n/c	A14		+3.3V	A45		AD[52]	A76
GND	B15		GND	B46		AD[51]	B77
RST#	A15		AD[13]	A46		AD[50]	A77
CLK	B16		AD[12]	B47		AD[49]	B78
n/c	A16		AD[11]	A47		GND	A78
GND	B17		AD[10]	B48		n/c	B79
GNT#	A17		GND	A48		AD[48]	A79
REQ#	B18		M66EN	B49		AD[47]	B80
GND	A18		AD[09]	A49		AD[46]	A80
n/c	B19		GND	B50		AD[45]	B81
n/c	A19		GND	A50		GND	A81
AD[31]	B20		GND	B51		GND	B82
AD[30]	A20		GND	A51		AD[44]	A82
AD[29]	B21		AD[08]	B52		AD[43]	B83
+3.3V	A21		C/BE[0]#	A52		AD[42]	A83
GND	B22		AD[07]	B53		AD[41]	B84
AD[28]	A22		+3.3V	A53		n/c	A84
AD[27]	B23		+3.3V	B54		GND	B85
AD[26]	A23		AD[06]	A54		AD[40]	A85
AD[25]	B24		AD[05]	B55		AD[39]	B86
GND	A24		AD[04]	A55		AD[38]	A86

PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #
+3.3V	B25		AD[03]	B56		AD[37]	B87
AD[24]	A25		GND	A56		GND	A87
C/BE[3]#	B26		GND	B57		n/c	B88
IDSEL	A26		AD[02]	A57		AD[36]	A88
AD[23]	B27		AD[01]	B58		AD[35]	B89
+3.3V	A27		AD[00]	A58		AD[34]	A89
GND	B28		n/c	B59		AD[33]	B90
AD[22]	A28		n/c	A59		GND	A90
AD[21]	B29		ACK64#	B60		GND	B91
AD[20]	A29		REQ64#	A60		AD[32]	A91
AD[19]	B30		+5V	B61		reserved	B92
GND	A30		+5V	A61		reserved	A92
+3.3V	B31		+5V	B62		reserved	B93
AD[18]	A31		+5V	A62		GND	A93
AD[17]	B32		Reserved	B63		GND	B94
AD[16]	A32		GND	A63		Reserved	A94
C/BE[2]#	B33		GND	B64			
+3.3V	A33		C/BE[7]#	A64			

Table 3-10: PCI/PCI-X Connector Pin Assignment and Interface Signals

3.11 AvBus DAUGHTER CARDS

AvBus daughter cards interface to the Virtex-II Development backplane general I/O, memory expansion, and auxiliary interface AvBus connectors. Power sources for the daughter cards are switchable to allow the card to be powered as a stand-alone unit as well powered via the backplane when installed.

The AvBus daughter cards address the need for expansion and scalability by offering modular designs using industry-leading components such as IP cores, drivers, applications code, development software, as well as test and analysis tools. These modules can be added to the platform via the six (P2, P3, P4, P5, P6 & P7 – P6 & P7 are available only with FF1152 package) AvBus connectors stated above.

3.12 EVALUATION BOARDS

Evaluation boards primary purpose is being used as a stand-alone integration/evaluation tool. However, the evaluation board pin-out is common to that of the backplane in the event integration between the two platforms is desired. Evaluation boards interface to the Virtex-II Development backplane via the AvBus interfaces connector. Power sources for the module are switch able to allow the card to be powered as a stand-alone unit as well powered via the backplane when installed.

3.13 EXTENDER CARD BOARD

Provisions for an extender card interface may be incorporated on the development modules or boards, which have the same pin assignment as the backplane connectors. This allows breakout capability of all connector signals for evaluation.

3.14 CONFIGURATION CODES

Upon power-up the FPGA will be enabled in a configuration mode defined by jumper header JP1. The default configuration mode is "Master-Serial" mode, which will allow the FPGA to be programmed from the System ACE MPM. The System ACE has been programmed with a simple test code that will enable LED scanning and basic UART communication. Table 3-11 describes the various configuration modes available by setting the appropriate jumper/mode select.

Configuration Mode	M2 JP1 (1-2)	M1 JP1 (3-4)	M0 JP1 (5-6)
* Master serial	OPEN	OPEN	OPEN
Slave serial	JUMPERED	JUMPERED	JUMPERED
Master SelectMAP	OPEN	JUMPERED	JUMPERED
Slave SelectMAP	JUMPERED	JUMPERED	OPEN
Boundary-scan	JUMPERED	OPEN	JUMPERED

* = Default assembled state

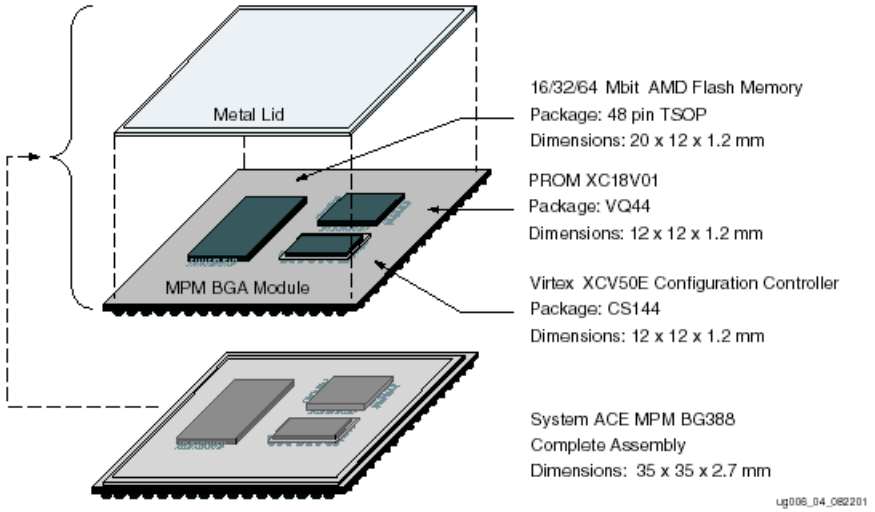
Table 3-11: Virtex-II Power-up Configuration Codes

Appendix A:

See the following pages for detailed information on using the SystemACE on the Virtex-II Development Platform.

Using the SystemACE on the Virtex-II Dev Platform

The Avnet Virtex-II Development Platform uses the SystemACE MPM storage solution, instead of proms to store the Virtex-II's configuration files. The MPM solution consists of an 18V01 prom, Virtex-E 50, and a 64Mbit AMD flash device.



Please see http://www.xilinx.com/isp/systemace/systemacempm.htm for more information on the SystemACE MPM.

Preparing MPM File

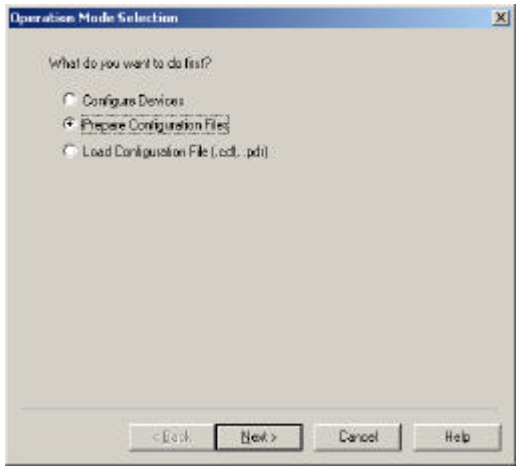
Prior to performing this step, bit files must have been created for each design using the CCLK option.

Start File Generation Mode of iMPACT by either

1. Selecting "Prepare Configuration Files" when launching iMPACT.

or

2. Use "Mode" pull-down or icon. Right-click white space to start wizard.

a. 

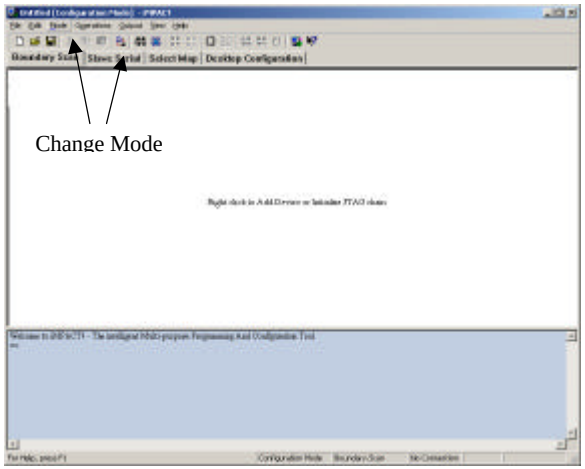
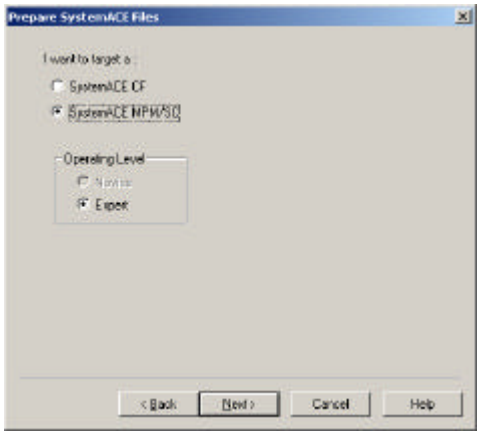
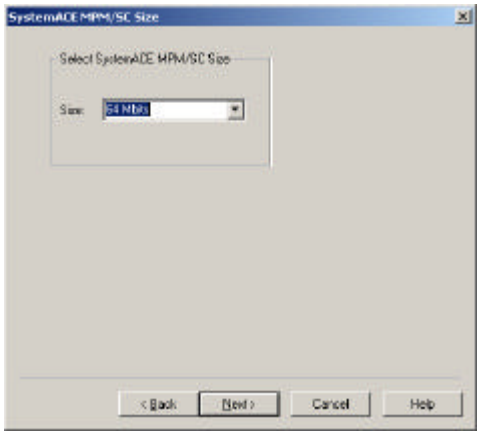
b. 

Figure 1 File Generation Mode

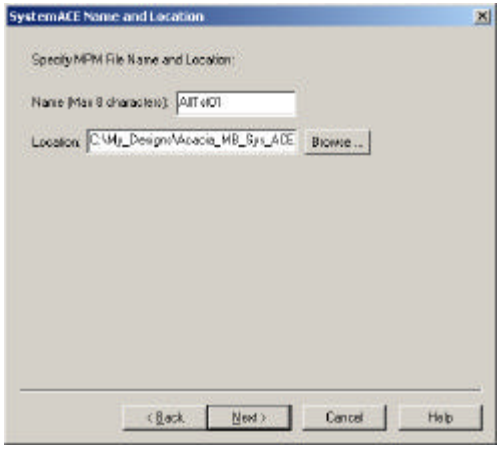
Select "**SystemACE File**" and click **Next**.
Select "**SystemACE MPM/SC**" and click **Nex**t.



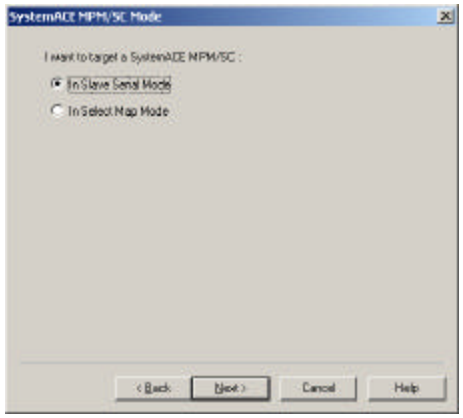
Select size of **64 Mbits** and click **Next**.



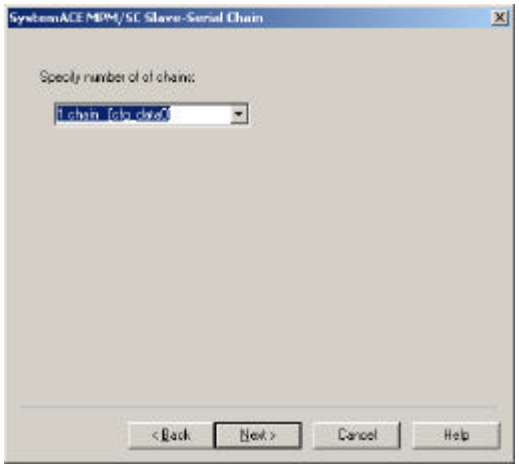
Give the file a name, and specify the desired location.



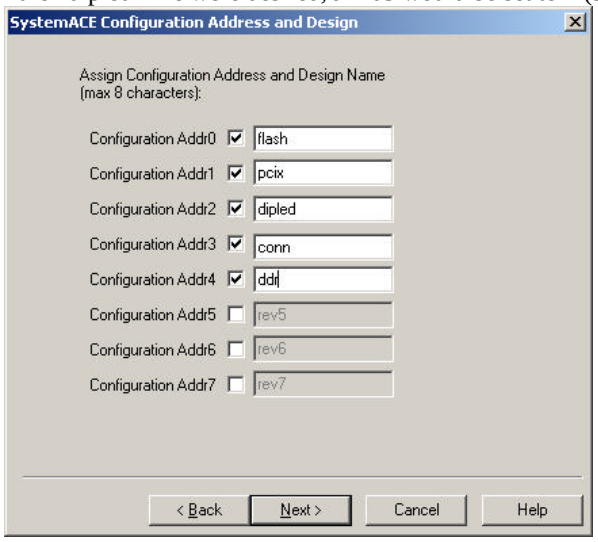
Select the desired mode (our example uses **Slave Serial**).



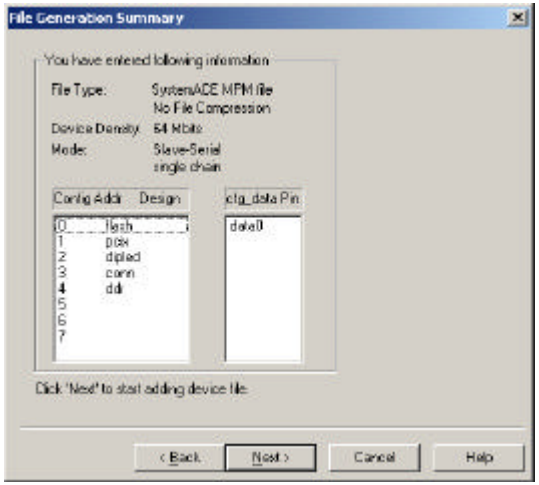
Select number of chains (our board has **1 chain**, using **data0**).



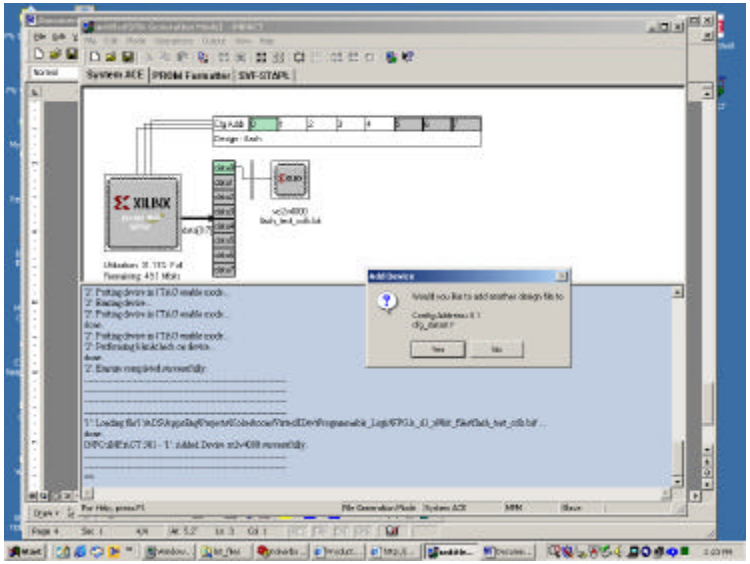
Select the number of design files that will be in the MPM file by checking the corresponding box. Note that for each design, you will be asked for a bit file later in this process. For each chain (our example uses 1 chain), you may have multiple design files (our ex. uses 5 design files) that can be loaded. These are jumper selectable on our board using JP103 and correspond to the Configuration Addr. In the example below, if the "dipled" file were desired, JP103 would be set to 2 (shunt on pins 3-4).



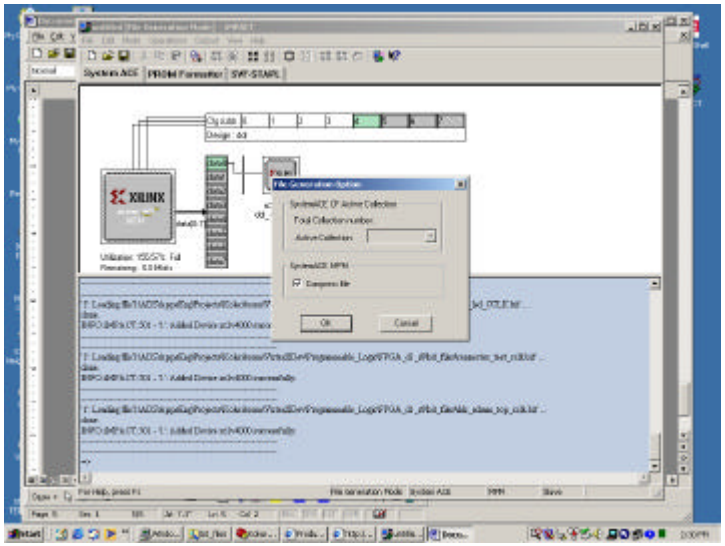
After clicking Next, a file generation summary will be presented. If all is satisfactory, press Next to continue. The example below indicates that our MPM file will have 5 designs (we will provide a bit file for each) and load via Slave-Serial mode with data0.



When prompted for a design file for config address 0, add the first bit bit file. The tool will ask if another file is to be added to config address 0. Select No. The tool will then move on to config address 1. Add the second bit file. Continue until a bit file has been assigned to each config address. Note that these bit files should have been previously built using the CCLK option.



In our case, the total size of the file exceeded the capacity of the storage device. Note the utilization below at 155.57%. For this reason, we selected **Compress file** when prompted by the **File Generation Option window**.



Erasing the SystemACE

The SystemACE uses a 64Mbit flash device which must be erased prior to programming. To do so, iMPACT will issue an erase command to the flash, delay a given amount of time, and try to read back from the device to verify that it is blank (FF's). There are cases where the tool does not wait long enough, and the device isn't erased. It is recommended that a patch be installed in the Xilinx install directory as follows:
%XILINX%**acempm**\data\impact.acd
Be sure to replace the one in the **acempm** directory!
This will replace the impact.acd file and extend the wait time for iMPACT from 2 to 3 minutes.

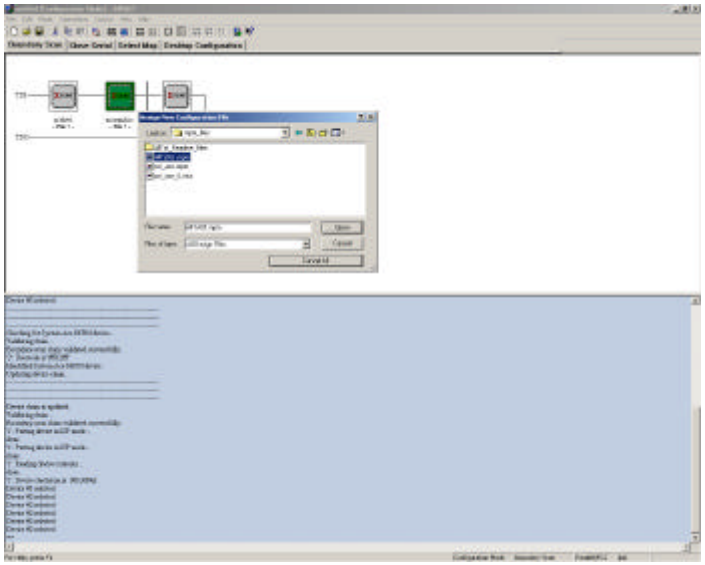
1. After initializing the jtag chain, right-click on the SystemACE device (2nd in the chain).
2. Select Erase.
3. The tool will seem to hang. It is actually waiting for the flash to erase. This should take approximately 3 minutes.
4. If the tool reports a successful erase, proceed to the programming section of this document.

When iMPACT fails to erase the device, it reports a "part is not blank" error. It will try again, but if it failed the first time, it is not going to pass on the second try. It is better to exit the tool completely and try again.

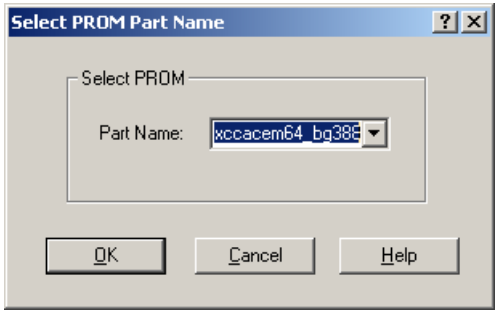
Programming the SystemACE

!Important! The following procedure assumes that the device was successfully erased prior to this step.

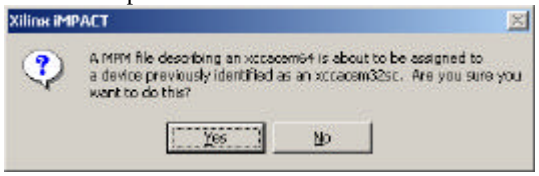
Initialize the jtag chain using iMPACT.
Right-click the xccace device (2nd device in the chain) and select **Assign New Configuration File**.
Note: You **do not** need to assign a file to the 18V01!



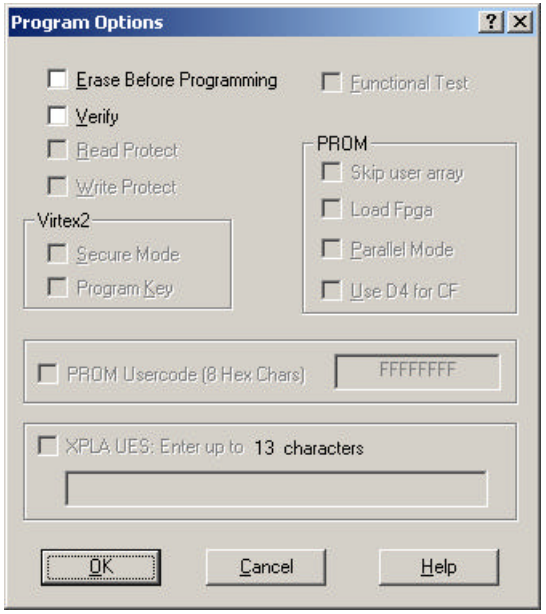
When prompted, select **xccace64_bg388**.



Impact will give the following warning. It is OK to ignore this. Click Yes to proceed.



Right-click the **xccace** device and select **program**.
De-select **Erase Before Programming**. This should have been previously erased. If the device was not previously erased, the tool will proceed to program, but will not function properly (the FPGA won't load).



Click OK to continue.
After programming, remove power and select the desired design file using JP103.
Apply power. D3 should indicate a high on FPGA done.