Table of Contents

Figures

Tables

Description:

The Communications/Memory Module is an expansion daughtercard for use with the Avalon Reference Design System™. The daughtercard interfaces via AvBus connectors and provides general-purpose resources to complement Avalon base modules. The daughtercard provides all necessary resources for implementation of Xilinx™ MicroBlaze™ core designs.

Features:

- 64 Mbytes SDRAM
- 16 Mbytes FLASH
- 1 Mbyte SRAM
- 10/100/1000 Ethernet PHY
- IrDA
- USB 2.0
- PC Card

Ordering Information:

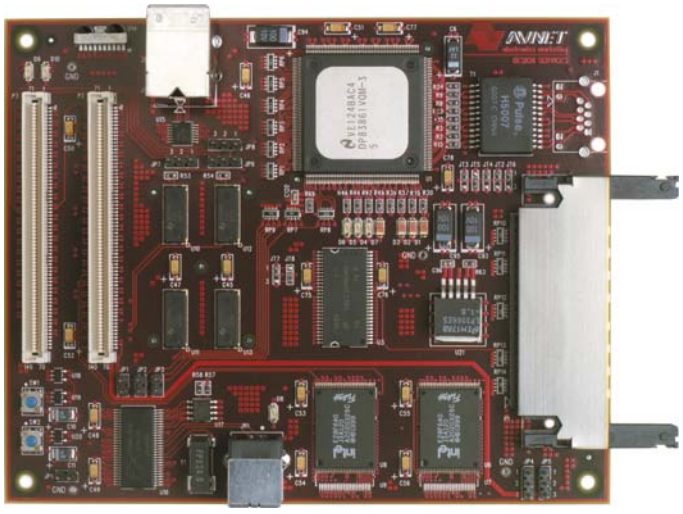
The following table lists the Module part numbers and available software options.

Internet Link at http://www.em.avnet.com/

Part Number	Description
ADS-EMU-DAU	Communications/Memory Module
ADS-XLX-MB-DAU	Communications/Memory Module bundled with MicroBlaze Core License

Target Applications:

- Complete resources for implementation of Xilinx MicroBlaze Core
- Functional expansion of Avalon Reference Design System evaluation and development kits
- Ethernet 10/100/1000 interface
- PC Card development
- USB 2.0 applications



1.0 Overview

The Communications/Memory Module is a daughterboard, which provides additional memory resources and communications capabilities to motherboards, which are compliant with the Avnet Design Services Avalon Reference Design System™. In particular, this module will focus on providing the memory subsystems needed for demonstration of the Xilinx MicroBlaze™ core and a peripheral set which demonstrates the versatility of the Virtex™-E and Virtex-II FPGA families. The module provides the following resources:

- 64 Mbytes SDRAM
- 16 Mbytes FLASH
- 1 Mbyte SRAM
- 10/100/1000 Ethernet PHY
- IrDA
- USB 2.0
- PC Card

2.0 Capabilities Matrix

While the Communications/Memory Module is intended to be used by any motherboard compliant with the Avalon Reference Design System™, the design has been optimized for the Avnet Xilinx™ Virtex-II Development board, the Avnet Xilinx Spartan®-IIE Evaluation board and the Avnet Xilinx Virtex-E Development board. Various combinations of resources are available depending on which board the module is supporting, the FPGA installed on the motherboard and how it is attached.

The Communications/Memory Module can be connected to the Virtex-II Development board, the Spartan-IIE Evaluation board or the Virtex-E Development board in two ways. The first, the normal connection, has both AvBus connectors on the motherboard connected with both AvBus connectors on the module. The other method, the offset connection, has only one of the AvBus connectors used on each board.

Normal (2 connector)
Xilinx Virtex-II Development Board P5 to Communications/Memory Module J4
Xilinx Virtex-II Development Board P4 to Communications/Memory Module J3

Xilinx Spartan-IIE Evaluation Board P2 to Communications/Memory Module J4
Xilinx Spartan-IIE Evaluation Board P1 to Communications/Memory Module J3

Xilinx Virtex-E Development Board P12 to Communications/Memory Module J4
Xilinx Virtex-E Development Board P11 to Communications/Memory Module J3

Offset (1 connector)
Xilinx Virtex-II Development Board P4 to Communications/Memory Module J4
Xilinx Virtex-II Development Board P5 No Connect
Communications/Memory Module J3 No Connect

Xilinx Spartan-IIE Evaluation Board P1 to Communications/Memory Module J4
Xilinx Spartan-IIE Evaluation Board P2 No Connect
Communications/Memory Module J3 No Connect

Xilinx Virtex-E Development Board P11 to Communications/Memory Module J4
Xilinx Virtex-E Development Board P12 No Connect
Communications/Memory Module J3 No Connect

The Xilinx Virtex-II Development Board can be assembled with either an XC2V1500, XC2V2000 in the FF856 package, or an XC2V4000-10000 in the FF1152 package.

The table below shows the combinations of part type and connection versus the resources available to the motherboard from the Communications/Memory Module.

	SDRAM	SRAM	Flash	GbE	IrDA	USB	PCCard	Notes
Xilinx Virtex-II Development Board 1500, FF896, Normal	X	X	X	X	X			
Xilinx Virtex-II Development Board 1500, FF896, Offset				X	X	X	X	
Xilinx Virtex-II Development Board 2000, FF896, Normal	X	X	X	X	X		X	
Xilinx Virtex-II Development Board 2000, FF896, Offset				X	X	X	X	
Xilinx Virtex-II Development Board 4000+, FF1152, Normal	X	X	X	X	X	X	X	
Xilinx Virtex-II Development Board 4000+, FF1152, Offset				X	X	X	X	
Xilinx Spartan-IIE Evaluation Board Normal	X	X	X	X	X			
Xilinx Spartan-IIE Evaluation Board Offset				X	X	X		
Xilinx Virtex-E Development Board Normal	X	X	X	X	X		X	
Xilinx Virtex-E Development Board Offset				X	X	X	X	

Table 2-1: Capabilities Matrix

3.0 Block Diagram

The following diagram displays the hardware for Communications/Memory Module.

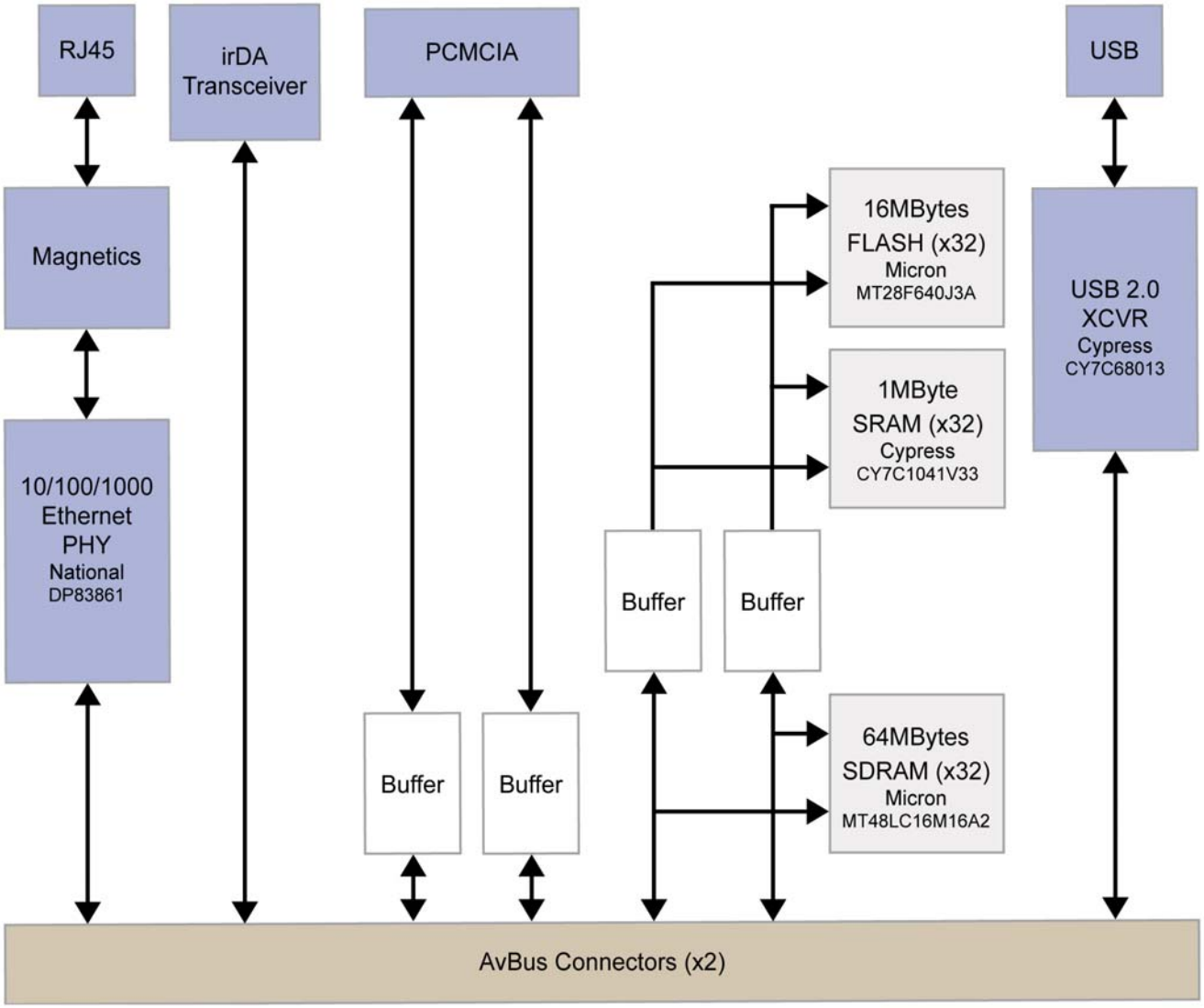


Figure 1: Communications/Memory Module Block Diagram

4.0 Mechanical

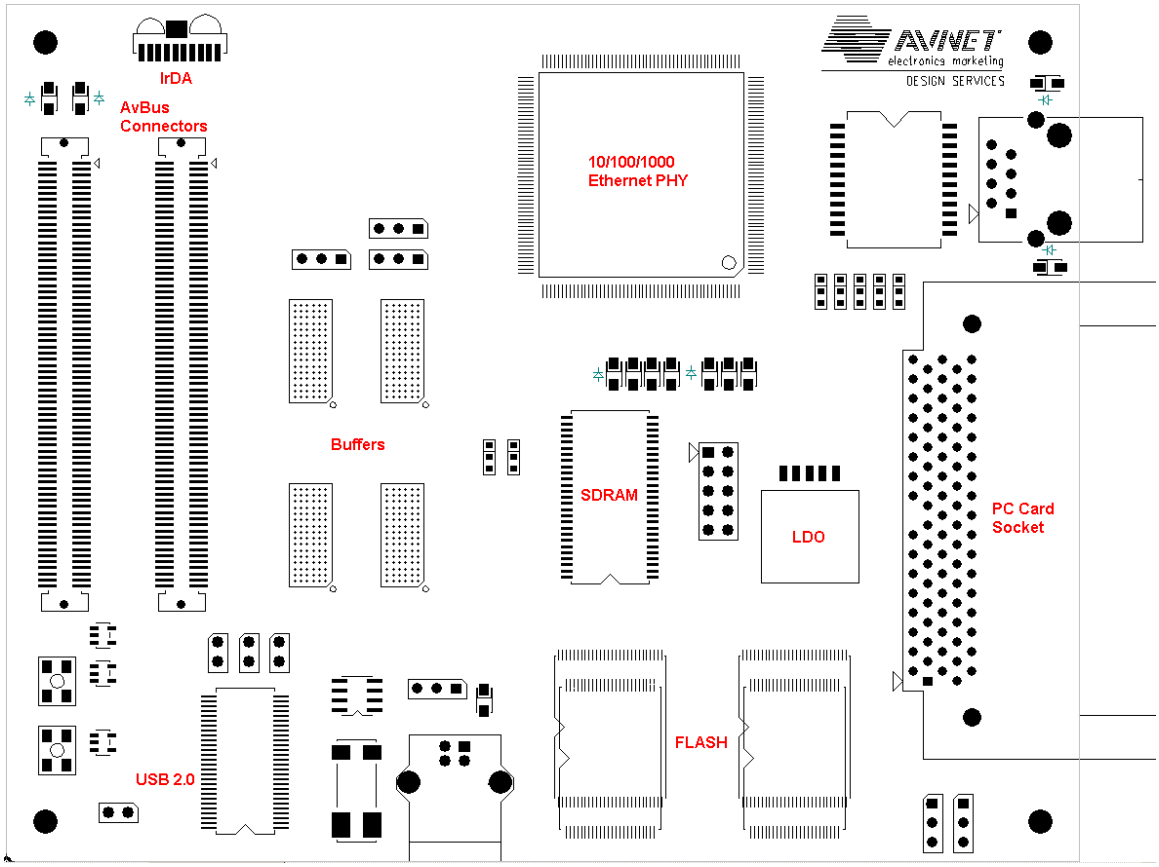


Figure 2: Part Placement – Top

Board Dimensions: 5.5" x 4.4"

The Communications/Memory Module Printed Circuit Board (PCB) is an eight-layer board, which has three signal layers, two ground planes and a +3.3V power plane. The board stack-up is as follows:

Layer 1: Primary Component
Layer 2: Ground Plane
Layer 3: Signal
Layer 4: Signal
Layer 5: Ground
Layer 6: Signal
Layer 7: +3.3VDC Power
Layer 8: Secondary Component

5.0 Memory Interfaces

5.1 AvBus

The memory is interfaced to the FPGA on the Virtex II development board or the Spartan II-E Evaluation board via the AvBus Memory with JTAG connector. This connector provides 32 bits of address bus, 32 bits of data bus, read/write, chip select, buffer control and memory control signals. The module buffers both the address and data buses from the AvBus connector before they are connected to the memory devices and the PCCard connector.

5.2 SDRAM

The module incorporates 64Mbytes of SDRAM organized as 16Mbits x 32. The two Micron MT48LC16M16A2 256Mbit SDRAM devices are connected directly to the AvBus connector (J3).

5.3 SRAM

The module incorporates 1Mbyte of SRAM organized as 256K x 32. The two Cypress CY7C1041V33 are connected to the address bus (U10) and data bus buffers (U11).

5.4 FLASH

The Module incorporates 16 Mbytes of FLASH memory organized as 4M x 32. The two flash devices are connected to the address (U10) and data buffers (U11). The PCB is designed so that the footprint patterns for the two types of FLASH are overlaid. This allows the use of either (2) Intel E28F640J3 (U6, U8), (2) Micron MT28F640J3 (U6, U8) or (2) AMD Am29LV640DU (U7, U9). Either part can be installed at assembly time. Due to reliability issues with sockets, the Flash devices are mounted directly to the PCB and JTAG tools are used for programming.

6.0 Communication Interfaces

6.1 I/O Interfaces

The Communications/Memory Module provides several I/O interfaces:

- Gigabit Ethernet
- USB 2.0
- IrDA
- PCMCIA/PCCard

6.1.1 Gigabit Ethernet

The Communications/Memory Module contains a National Semiconductor DP83861 Gigabit Ethernet PHY. This PHY implements a GMII interface to connect to the FPGA via AvBus connector (J4) and supports a Gigabit Ethernet Over Copper interface on the media side. The PHY is connected to the appropriate magnetics module, which connects to an RJ45 connector. The PHY supports Gigabit Ethernet via the GMII interface and 10/100 Mbps Ethernet via the subset MII interface.

Nine LEDs are included on the board, two of them in the RJ45 connector (J1). The two LEDs in the RJ45 connector indicate LINK and ACTIVITY. The other seven LEDs on the board indicate RX ACTIVITY (D1), TX ACTIVITY (D2), COLLISION (D3), 1000 Mbps (D4), 100 Mbps (D5), 10 Mbps (D6) and DUPLEX (D7).

The initial configuration of the PHY is determined by the logic level present on six pins during POReset. The logic levels on these pins are determined by the installation of 1K resistor jumpers during assembly. The following table lists the configuration options:

JT1	JT2	JT3	JT4	JT5	JT6	Function
1-2						Reference clock set to 25 MHz
2-3						Reference clock set to 125 MHz
	1-2					Disables Non-compliant mode
	2-3					Enables Non-compliant mode
		1-2				Configures PHY to Slave during Master/Slave negotiation
		2-3				Configures PHY to Master during Master/Slave negotiation
			1-2			Disables Manual Master/Slave configuration
			2-3			Enable Manual Master/Slave configuration
				1-2		Disables Auto-negotiation
				2-3		Enables Auto-negotiation
					1-2	Advertises Single-Node
					2-3	Advertises Multi-Node

Table 6-1: Gigabit Ethernet Configuration Options

A 25 MHz crystal oscillator (U22) is installed on the board to provide the reference clock to the PHY. However, some MACs require that the PHY run off of their reference clock. The selection of the 25 MHz reference clock for the PHY is provided by the installation of zero ohm jumpers as follows:

JT9	Function
1-2	Reference clock provided by MAC
2-3	Reference clock provided by on-board crystal oscillator

Table 6-2: Reference Clock Selection

6.1.2 IrDA

An Agilent HSDL-3600 IrDA transceiver is included on the board. This transceiver provides IrDA 1.1 compliant links from 9.6 kbps to 4Mbps. It is connected to the FPGA via the AvBus connector (J4).

When connected to the Spartan-IIE Evaluation board in the normal configuration, the Mode 0, Mode 1 and FIR Select pins of the transceiver are not driven by the FPGA. In this case, these pins are controlled by the installation of 4.7 K ohm resistor jumpers as follows:

JT11	JT12	JT13	Function
1-2			FIR Select = SIR
2-3			FIR Select = MIR/FIR
	1-2		Mode 1 = 0
	2-3		Mode 1 = 1
		1-2	Mode 0 = 0
		2-3	Mode 0 = 1

Table 6-3: IrDA Mode Select Settings

6.1.3 PCMCIA/PCCard

A PC Card connector is incorporated on the board and connected to the FPGA via the AvBus connector (J4). The PC Card connector (P1) supports 26 address lines and 16 data lines. These address and data lines are buffered separately from the memory address and data busses (U12, U13). The socket does not support hot swapping. The Vcc and Vpp pins are selectable via jumpers (JP4, JP5) between +3.3 Vdc and +5 Vdc.

6.1.4 USB

A Cypress CY7C68013 single chip USB 2.0 compliant transceiver is incorporated on the board. This transceiver can support data transfers up to the maximum USB 2.0 defined data rate of 56 Mbytes per second as well as handling both USB 1.1 and USB 2.0 defined protocols. The transceiver operates at Full Speed (12 Mbps) and High Speed (480 Mbps). The part is connected to a USB Type B connector (JR1). An LED (D8) indicates link power although the transceiver is powered by the +3.3V board power plane. Two pushbutton switches are included on the board to generate Reset (SW1) and WakeUp (SW2). The data path and control interfaces are connected to the FPGA via the AvBus connector (J4).

7.0 Connectors

7.1 AvBus

Avnet Design Services has defined four configurations for the AvBus connector. Two of those configurations are used in the Communication/Memory Module; AvBus Memory with JTAG and AvBus Memory without JTAG. The pin definitions for these connectors on the Communications/Memory Module are as follows:

Pin	AvBus Spec Signal Name	Function		Pin	AvBus Spec Signal Name	Function
1	**+5Vdc**			71	Addr0	A0
2	Addr1	A1		72	**Gnd**	
3	Addr2	A2		73	Addr3	A3
4	**Gnd**			74	Addr4	A4
5	Addr5	A5		75	**Gnd**	
6	Addr6	A6		76	Addr7	A7
7	**Gnd**			77	Addr8	A8
8	Addr9	A9		78	**+3.3Vdc**	
9	Addr10	A10		79	Addr11	A11
10	**Gnd**			80	Addr12	A12
11	Addr13	A13		81	**Gnd**	
12	Addr14	A14		82	Addr15	A15
13	**+5Vdc**			83	Addr16	A16
14	Addr17	A17		84	**Gnd**	
15	Addr18	A18		85	Addr19	A19
16	**Gnd**			86	Addr20	A20
17	Addr21	A21		87	**Gnd**	
18	Addr22	A22		88	Addr23	A23
19	**Gnd**			89	Addr24	A24
20	Addr25	A25		90	**+3.3Vdc**	
21	Addr26	A26		91	Addr27	A27
22	**Gnd**			92	Addr28	A28
23	Addr29	A29		93	**Gnd**	
24	Addr30	A29		94	Addr31	A31
25	**+5Vdc**			95	Data0	D0
26	Data1	D1		96	**Gnd**	
27	Data2	D2		97	Data3	D3
28	**Gnd**			98	Data4	D4
29	Data5	D5		99	**Gnd**	
30	Data6	D6		100	Data7	D7
31	**Gnd**			101	Data8	D8

Pin	AvBus Spec Signal Name	Function		Pin	AvBus Spec Signal Name	Function
32	Data9	D9		102	**+3.3Vdc**	
33	Data10	D10		103	Data11	D11
34	**Gnd**			104	Data12	D12
35	Data13	D13		105	**Gnd**	
36	Data14	D14		106	Data15	D15
37	**+5Vdc**			107	Data16	D16
38	Data17	D17		108	**Gnd**	
39	Data18	D18		109	Data19	D19
40	**Gnd**			110	Data20	D20
41	Data21	D21		111	**Gnd**	
42	Data22	D22		112	Data23	D23
43	**Gnd**			113	Data24	D24
44	Data25	D25		114	**+3.3Vdc**	
45	Data26	D26		115	Data27	D27
46	**Gnd**			116	Data28	D28
47	Data29	D29		117	**Gnd**	
48	Data30	D30		118	Data31	D31
49	**+5Vdc**			119	Flash_CE0#	Flash_CS#
50	Flash_CE1#	SRAM_CS#		120	**Gnd**	
51	Flash_OE#	OE#		121	Flash_WE#	WE#
52	**Gnd**			122	Flash_Reset#	RST#
53	SDRAM_CS#	SDRAM_CS#		123	**Gnd**	
54	SDRAM_CAS#	CAS#		124	SDRAM_WE#	MDBUF_DIR
55	**Gnd**			125	SDRAM_Clk	CLK
56	SDRAM_RAS#	RAS#		126	**+3.3Vdc**	
57	SDRAM_ClkEn	CLKEN		127	SDRAM_Byte0#	BS0#
58	**Gnd**			128	SDRAM_Byte1#	BS1#
59	SDRAM_Byte2#	BS2#		129	**Gnd**	
60	SDRAM_Byte3#	BS3#		130	User_I/O0	PCCDBUF_OE#
61	**+5Vdc**			131	User_I/O1	PCCDBUF_DIR
62	User_I/O2	MDBUF_OE#		132	**Gnd**	
63	User_I/O3	N/C		133	User_I/O4	MABUF_OE#
64	**Gnd**			134	User_I/O5	PCCABUF_OE#
65	User_I/O6	N/C		135	**Gnd**	
66	User_I/O7	N/C		136	User_I/O8	N/C
67	**Gnd**			137	TMS	SEC_TMS
68	TDO	SEC_TDO		138	**+3.3Vdc**	
69	TCK	SEC_TCK		139	TDI	SEC_TDI
70	**Gnd**			140	TRST	SEC_TRST#

Table 7-1: AvBus Memory Connector (with JTAG)

Pin	AvBus Spec Signal Name	Function		Pin	AvBus Spec Signal Name	Function
1	**+5Vdc**			71	Data32	GMII_MDC
2	Data33	GMII_MDIO		72	**Gnd**	
3	Data34	GMII_COL		73	Data35	GMII_CRS
4	**Gnd**			74	Data36	GMII_RX_CLK
5	Data37	GMII_RX_ER		75	**Gnd**	
6	Data38	GMII_RXD7		76	Data39	GMII_RX_DV
7	**Gnd**			77	Data40	GMII_RXD6
8	Data41	GMII_RXD5		78	**+3.3Vdc**	
9	Data42	GMII_RXD3		79	Data43	GMII_RXD4
10	**Gnd**			80	Data44	GMII_RXD2
11	Data45	GMII_RXD1		81	**Gnd**	
12	Data46	GMII_TX_CLK		82	Data47	GMII_RXD0
13	**+5Vdc**			83	Data48	GMII_TX_ER

Pin	AvBus Spec Signal Name	Function		Pin	AvBus Spec Signal Name	Function
14	Data49	GMII_TX_EN		84	**Gnd**	
15	Data50	GMII_TXD6		85	Data51	GMII_TXD7
16	**Gnd**			86	Data52	GMII_TXD5
17	Data53	GMII_TXD4		87	**Gnd**	
18	Data54	GMII_TXD2		88	Data55	GMII_TXD3
19	**Gnd**			89	Data56	GMII_GTC_CLK
20	Data57	GMII_TXD0		90	**+3.3Vdc**	
21	Data58	GMII_TXD1		91	Data59	GBEINT#
22	**Gnd**			92	Data60	GBE_RST#
23	Data61	IRDA_D0		93	**Gnd**	
24	Data62	IRDA_MD1		94	Data63	PCC_REG#
25	**+5Vdc**			95	Flash_CE2#	KBDATA
26	Flash_CE3#	IRDA_TXD		96	**Gnd**	
27	SDRAM_Byte4#	IRDA_RXD		97	SDRAM_Byte5#	KBCLK
28	**Gnd**			98	SDRAM_Byte6#	MSDATA
29	SDRAM_Byte7#	MSCLK		99	**Gnd**	
30	User_I/O0	PT3 (see Notes)		100	User_I/O1	PT1 (see Notes)
31	**Gnd**			101	User_I/O2	PT2 (see Notes)
32	User_I/O3	PCC_CE2#		102	**+3.3Vdc**	
33	User_I/O4	PCC_CE1#		103	User_I/O5	PCC_WP
34	**Gnd**			104	User_I/O6	PCC_WAIT#
35	User_I/O7	USB_FD1		105	**Gnd**	
36	User_I/O8	USB_FD2		106	User_I/O9	PCC_CD1#
37	**+5Vdc**			107	User_I/O10	PCC_CD2#
38	User_I/O11	USB_FD3		108	**Gnd**	
39	User_I/O12	USB_FD4		109	User_I/O13	PCC_RDY_BSY
40	**Gnd**			110	User_I/O14	PCC_INPACK#
41	User_I/O15	USB_FD5		111	**Gnd**	
42	User_I/O16	USB_FD6		112	User_I/O17	PCC_BVD2
43	**Gnd**			113	User_I/O18	PCC_BVD1
44	User_I/O19	USB_FD7		114	**+3.3Vdc**	
45	User_I/O20	USB_FD8		115	User_I/O21	PCC_VS1
46	**Gnd**			116	User_I/O22	PCC_VS2
47	User_I/O23	USB_FD9		117	**Gnd**	
48	User_I/O24	USB_FD10		118	User_I/O25	USB_IFCLK
49	**+5Vdc**			119	User_I/O26	USB_CLKOUT
50	User_I/O27	USB_FD11		120	**Gnd**	
51	User_I/O28	USB_FD12		121	User_I/O29	USB_SLCS#
52	**Gnd**			122	User_I/O30	USB_PEND
53	User_I/O31	USB_FD13		123	**Gnd**	
54	User_I/O32	USB_FD14		124	User_I/O33	USB_FA0
55	**Gnd**			125	User_I/O34	USB_FA1
56	User_I/O35	USB_FD15		126	**+3.3Vdc**	
57	User_I/O46	USB_RDY0		127	User_I/O37	USB_FD0
58	**Gnd**			128	User_I/O38	USB_SLOE
59	User_I/O39	USB_RDY1		129	**Gnd**	
60	User_I/O40	USB_CTL0		130	User_I/O41	USB_WU2
61	**+5Vdc**			131	User_I/O42	GBE_MAC_25MHZ_CLK
62	User_I/O43	USB_CTL1		132	**Gnd**	
63	User_I/O44	USB_CTL2		133	User_I/O45	N/C
64	**Gnd**			134	User_I/O46	N/C
65	User_I/O47	USB_INT0#		135	**Gnd**	
66	User_I/O48	USB_INT1#		136	User_I/O49	N/C
67	**Gnd**			137	User_I/O50	N/C
68	User_I/O51	N/C		138	**+3.3Vdc**	
69	User_I/O52	N/C		139	User_I/O53	N/C
70	**Gnd**			140	User_I/O54	N/C

Table 7-2: AvBus Memory Connector (No JTAG)

Communications/Memory Module

by

Avnet Design Services

Avnet Design Services
Released

Rev 1.0 09/16/2002
Literature # ADS-002604

Notes:

JP9	JP8	JP7	Signal	Function
1-2			PT1	USB_INT0#
2-3			PT1	I2CSCL
	1-2		PT2	USB_INT1#
	2-3		PT2	I2CSDA
		1-2	PT3	USB_CTL2
		2-3	PT3	IRDA_FIR_SEL

Table 7-3: Jumper Table for Signals PT1, PT2 and PT3

7.2 USB Type B

Pin	Definition
1	+5 Vdc Line Power
2	Data-
3	Data+
4	Signal Gnd
5	Frame Gnd
6	Frame Gnd

Table 7-4: USB Type B Connector Assignment

7.3 Ethernet

Pin	Definition
1	Data A+
2	Data A-
3	Data B+
4	Data B-
5	Data C+
6	Data C-
7	Data D+
8	Data D-

Table 7-5: Ethernet RJ-45 Connector Assignment

8.0 Power Requirements

The two AvBus expansion connectors provide power for the circuits on the Expansion card. All devices on the expansion card operate at +3.3 volts. A National Semiconductor LP3966ES-1.8 LDO (U21) is used to generate the 1.8 volt core voltage supply for the Ethernet PHY. Input current requirements are TBD. Two LEDs indicate input power on the +3.3V (D9) and +5V (D10) power rails.