Linköpings universitet | Institutionen för systemteknik
Datablad | Datorteknik
2018

Laboration i digitalteknik

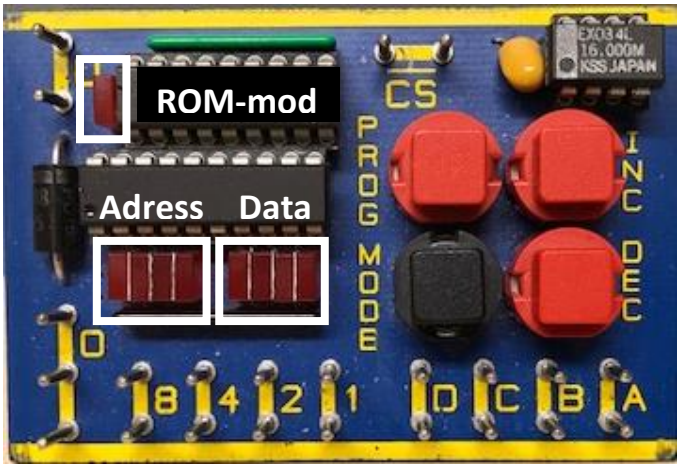
– Datablad

TSEA22 Digitalteknik D
TSEA51 Digitalteknik Y
TSEA52 Digitalteknik I
TDDC75 Diskreta strukturer IT

Linköpings universitet
SE-581 83 Linköping
013-28 10 00, www.liu.se

PROM-modul

Nedan visas en bild på PROM-modulen som innehåller ett läsminne.

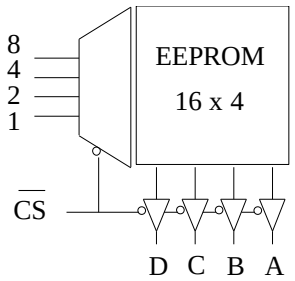


Läsminnet lagrar 16 stycken 4-bitsarsord och programmeras och raderas elektriskt (EEPROM). Kretsen har två moder, en programmeringsmod, PROG-mod, och en mod där modulens minne kan användas, ROM-mod. Växling mellan moderna sker genom att trycka på den svarta knappen markerad MODE. Lysdioden markerad ROM-mod lyser när kretsen är i ROM-moden.

I PROG-moden programmeras minnet med knapparna PROG, INC och DEC. Adress och tillhörande data visas på vardera 4 lysdioder. PROG-knappen används för att hoppa till nästa adress. Datainnehållet ändras med hjälp av knapparna INC (increase) och DEC (decrease). När önskat datainnehåll visas sparas detta genom att trycka på PROG-knappen. Minnet raderas genom att trycka på alla de 3 röda knappar samtidigt och som en indikering på detta växlas modulen över till ROM-moden.

I ROM-moden är minnesinnehållet fixerat och funktionen kan beskrivas av figuren nedan.

ROM - mode

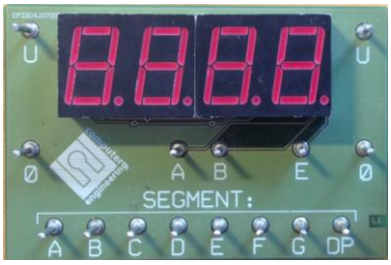


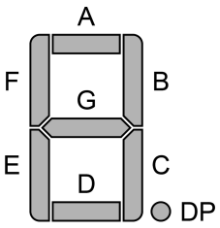
Pinnarna 8,4,2 och 1 är adressingångar där ingång 8 är mest signifikant bit och A-D datautgångar. I denna mod har modulen en speciell aktiveringssignal $\overline{CS}$ (Chip Select). $\overline{CS}$ = 0 innebär att utgångarna är aktiverade och $\overline{CS}$ = 1 bland annat att modulens utgångar inte är anslutna till minnets utgångar, dvs utgångarna är högohmiga. I ROM-moden visar lysdioderna adresserad minnescell och data på denna adress, förutsatt att chip select är aktiverad, dvs $\overline{CS}$ = 0.

LED-displayer

Oavkodad 7-segmentsdisplay

LED-modulen visas i figuren nedan.



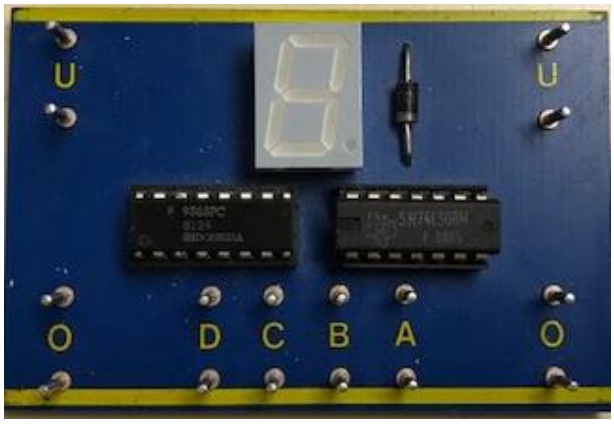


Modulen har fyra 7-segmentsdisplayer. Segmenten är namngivna A-G och DP står för decimalpunkt.

Med segmentingångarna A-G och DP väljs vilket eller vilka segment som skall vara tända. Ingångarna A och B direkt under displayerna används för att välja vilken av de fyra displayerna som skall tändas. Ingång A är minst signifikant bit och displayerna är numrerade i ordning 3, 2, 1 och 0. E står för enable och måste vara hög för att någon av displayerna överhuvudtaget ska lysa.

Avkodad 7-segmentsdisplay

Den avkodade 7-segmentsdisplayen visas i figuren nedan.



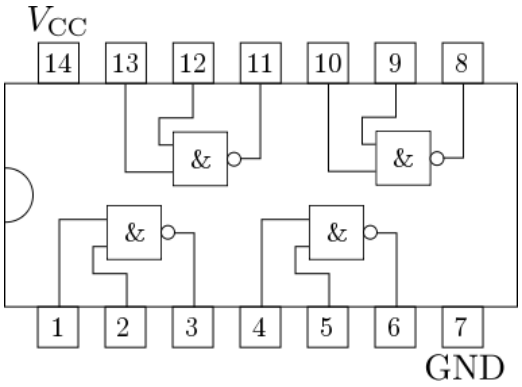
Displayen visar den hexadecimal siffra som svarar mot det binärkodade 4-bitarstal som matas in på ingångarna A-D där A är minst signifikant bit.

Klockpulsgenerator

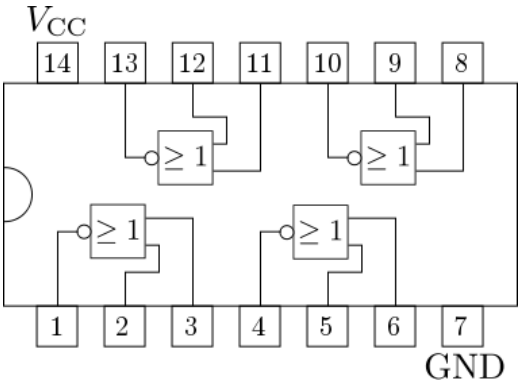
Figuren visar en klockpulsgenerator med variabel frekvens från 1 Hz – 1kHz.

Klockpulsen tas ut från OUT. Det finns tre frekvensintervall 1-10 Hz, 10-100 Hz och 100 -1000 Hz. Frekvensintervall väljas genom att koppla ihop den i figuren inringade pinnen med en av pinnarna markerade 1, 10 eller 100 Hz. Sedan justeras frekvensen inom valt intervall genom att justera den gula ratten på vridpotentiometern.

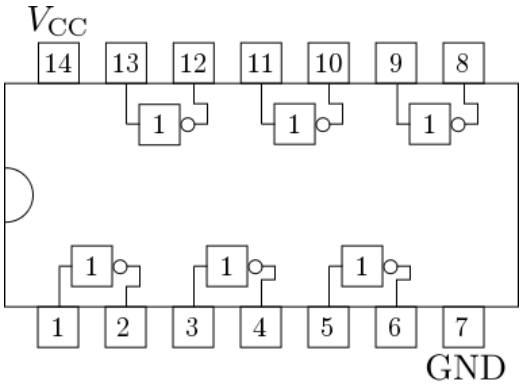
74LS00



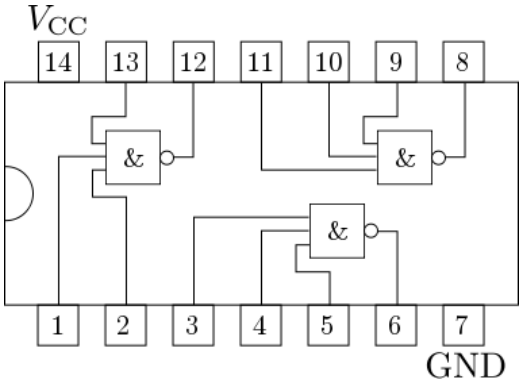
74LS02



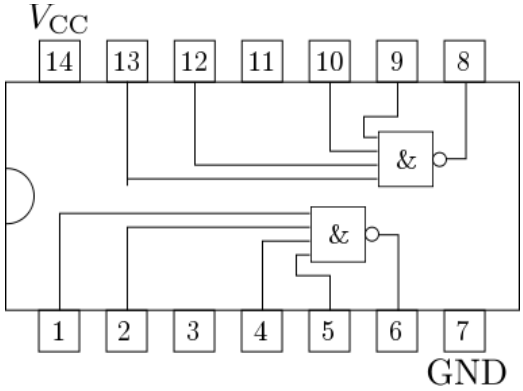
74LS04



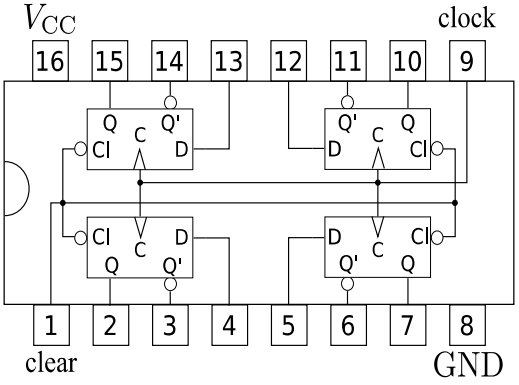
74LS10



74LS20



74LS175



National Semiconductor

June 1989

54LS153/DM54LS153/DM74LS153
Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

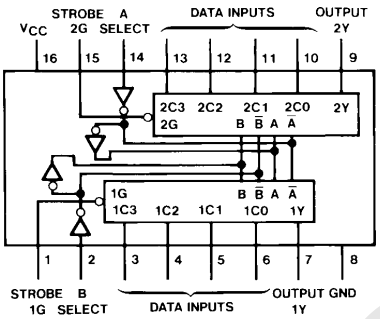
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  - — From data 14 ns
  - — From strobe 19 ns
  - — From select 22 ns
- Typical power dissipation 31 mW
- Alternate Military/Aerospace device (54LS153) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

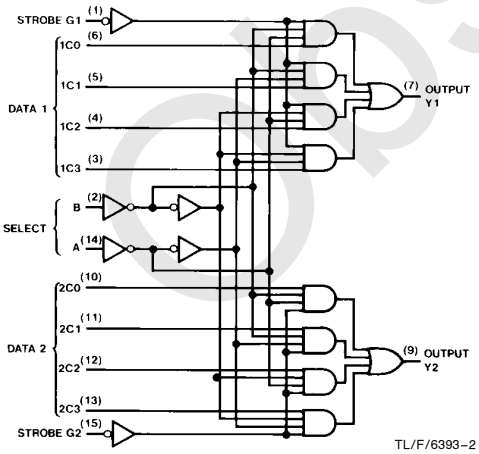
Dual-In-Line Package



TL/F/6393–1

Order Number 54LS153DMQB, 54LS153FMQB, 54LS153LMQB, DM54LS153J, DM54LS153W, DM74LS153M or DM74LS153N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Diagram



TL/F/6393–2

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

National Semiconductor

June 1989

54LS157/DM54LS157/DM74LS157, 54LS158/DM54LS158/DM74LS158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS157 presents true data whereas the LS158 presents inverted data to minimize propagation delay time.

Applications

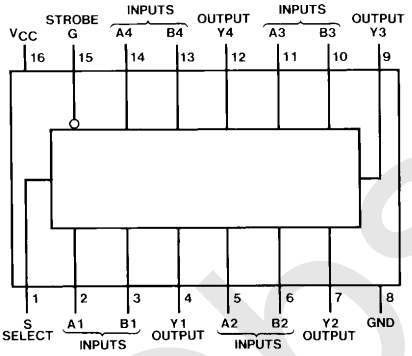
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Typical Propagation Time
  LS157 9 ns
  LS158 7 ns
- Typical Power Dissipation
  LS157 49 mW
  LS158 24 mW
- Alternate Military/Aerospace device (54LS157, 54LS158) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

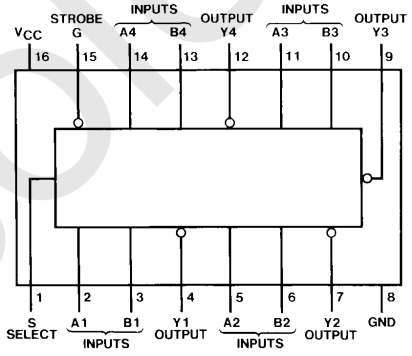
Dual-In-Line Package



TL/F/6396–1

Order Number 54LS157DMQB, 54LS157FMQB, 54LS157LMQB, DM54LS157J, DM54LS157W, DM74LS157M or DM74LS157N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



TL/F/6396–2

Order Number 54LS158DMQB, 54LS158FMQB, 54LS158LMQB, DM54LS158J, DM54LS158W, DM74LS158M or DM74LS158N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54162, SN54163, SN74160 THRU SN74163, SN74LS160A THRU SNLS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060

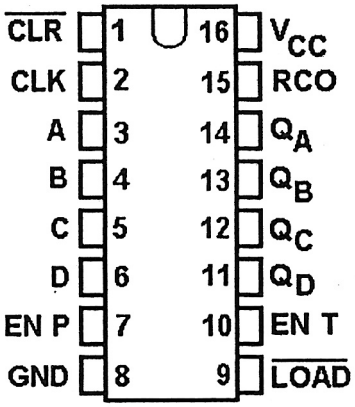
OCTOBER 1976 – REVISED MARCH 1988

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHZ	475 mW

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74', 74LS', 74S' . . . J OR N PACKAGE
(TOP VIEW)



description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function of the '160, '161, 'LS160A and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162 and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count lengths to be modified as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applicattions without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 or 'S163 are allowed regardless of the level of the clock input. The use of the ripple carry output as an edge trigger pulse is not recommended.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL}.

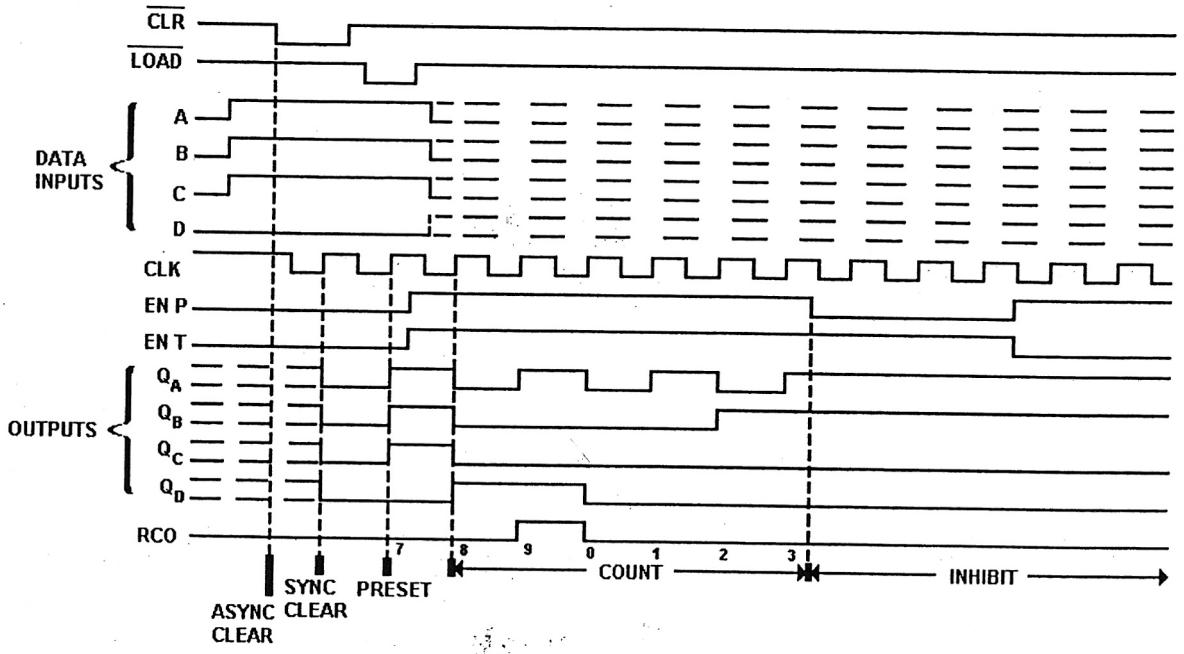
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

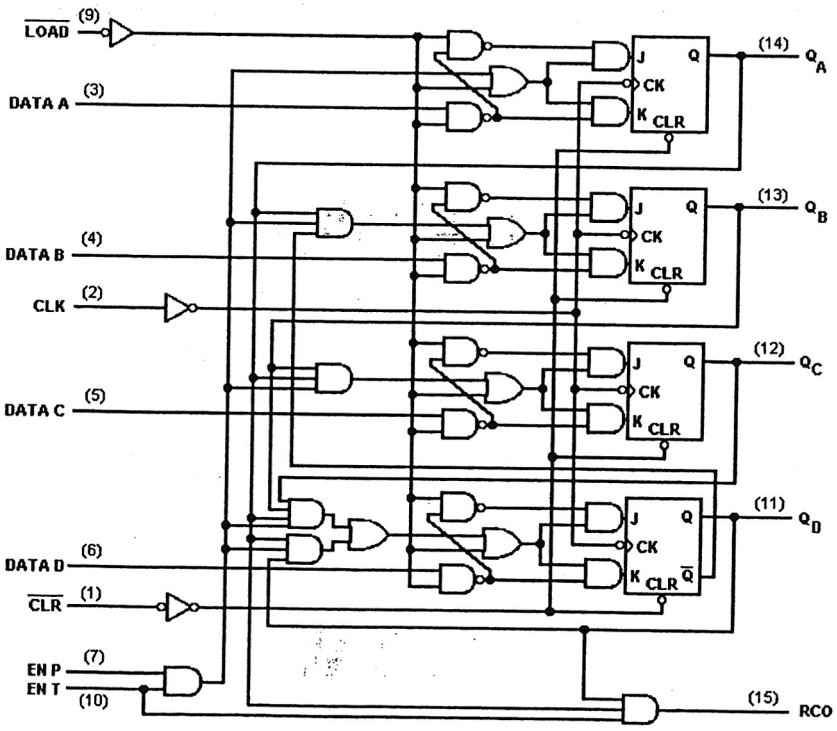
typical clear, preset, count and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two and three
4. Inhibit



logic diagram



SDLS192

TYPES SN54668, SN54LS669, SN74LS668, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

D2351, APRIL 1977 – REVISED MARCH 1988

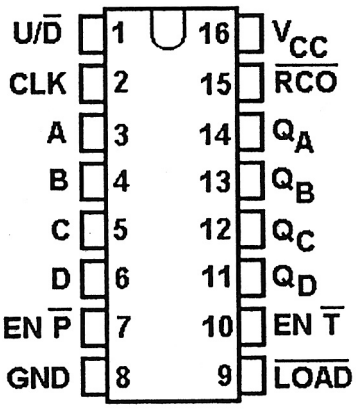
'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Buffered Outputs**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	35 MHz	35 MHz	100 mW

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74', 74LS', 74S' . . . J OR N PACKAGE
(TOP VIEW)



description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simulanteously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

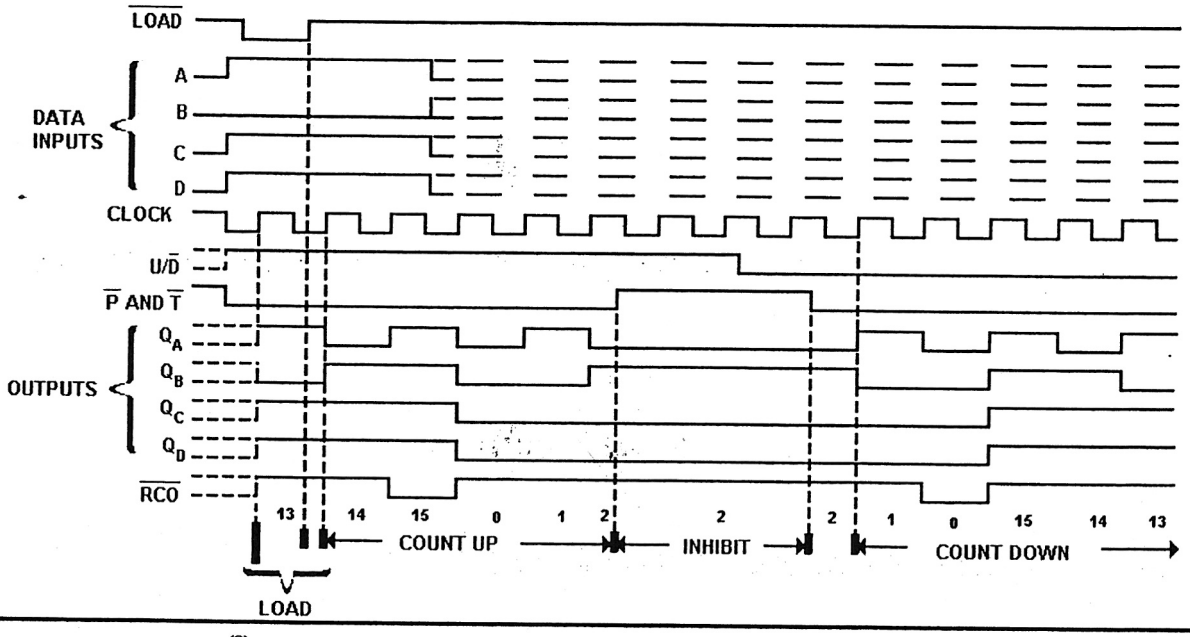
The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond hold time, reduced input currents I_{IH} and I_{IL} and all buffered outputs.

'LS669 BINARY COUNTERS

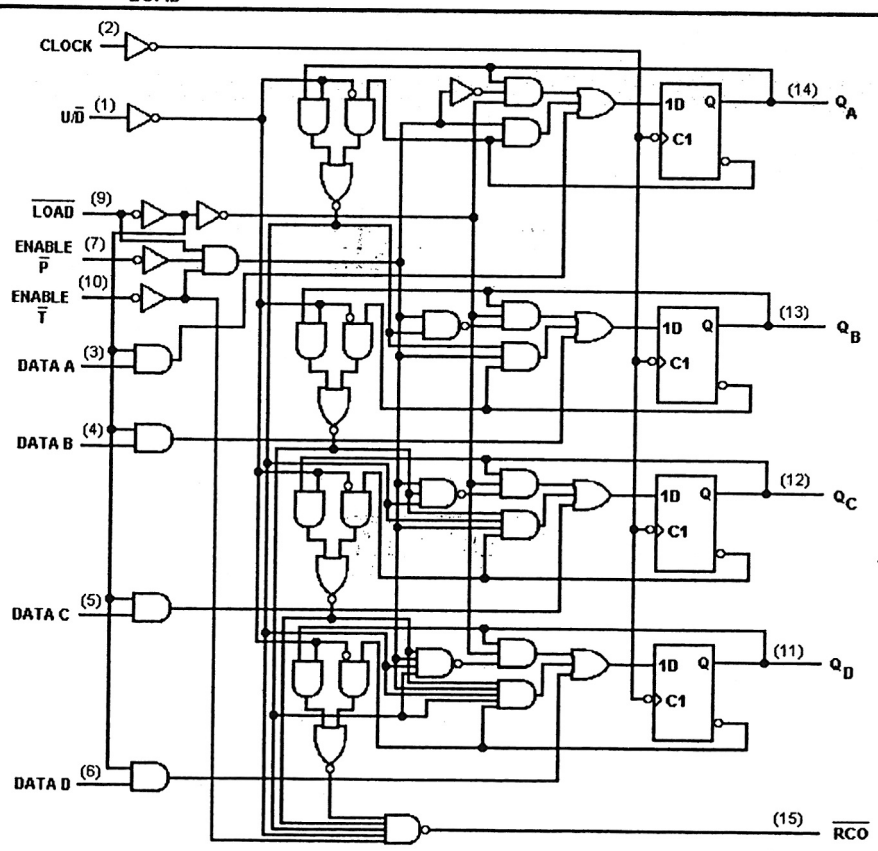
typical clear, preset, count and inhibit sequences

Illustrated below is the following sequence:

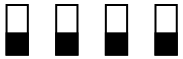
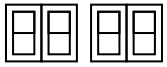
1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one and two
3. Inhibit
4. Count down to one, zero, (minimum), fifteen, fourteen and thirteen



logic diagram



Laborationsutrustning i Digitalteknik
Återställ modulerna enligt nedanstående karta

+5 0	 7-segment avkodad	 Skjutomkopplare	74LS00	74LS04	74LS153
+5 0	 7-segment avkodad	 Skjutomkopplare	74LS00	74LS10	74LS157
+5 0	 7-segment avkodad	Klockpulsgenerator	74LS00	74LS10	74LS160
+5 0	 7-segment	Minne	74LS00	74LS20	74LS160
+5 0	 Lysdioder	Minne	74LS02	74LS175	74LS160
+5 0	 Tryckomkopplare	Förgrening	74LS04	74LS175	74LS669