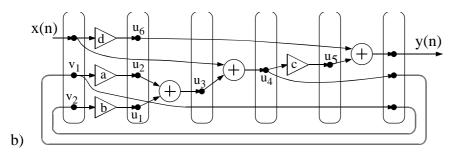
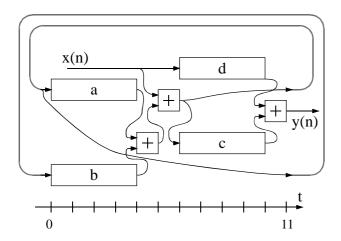
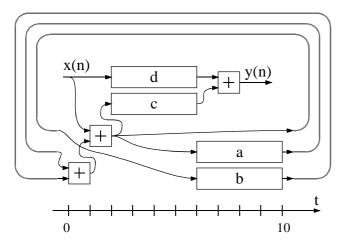
- 1. a) Binary offset representation is identical to two's complement except for the sign bit, which is inverted for binary offset compared to 2's complement. Converting from 2's complement to binary offset or the other way around is thus performed by inverting the sign bit.
 - b) Broadcast of memory values to all PEs simultaneiously, allow direct PE to PE communication, use interleaved memory access.
 - c) An heuristic optimization method is not guaranteed to generate the optimal solution. It is however possible to find solutions to large problems within resonable time, i.e., the comlpexity is polynomial.
 - d) A systolic array uses a global clock to synchronize the data exchange between the PE:s. A wavefront array does not have a global clock and uses handshaking to transmit data between processing elements.
 - e) The number of operations in an FFT implemented using 2 input butterflies uses $N/2 \log(N) = O(N \log N)$ butterfly operations where N is the number of points to perform the FFT on.
- 2. a) Tmin = max ((Tmult + Tadd + Tadd)/1, (Tmult + Tadd + Tadd)/2) = max (6, 3) = 6 time units.

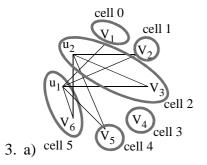


c) ALAP = As Late As Possible, move multiplication d to the right.



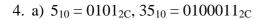
d) Move multiplication a and b to the left to shorten the critical path to be less than 10 time units. Let the last addition move one time unit to the right to simplify drawing.

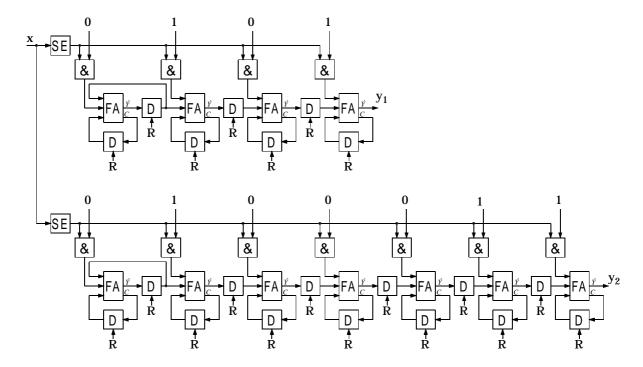




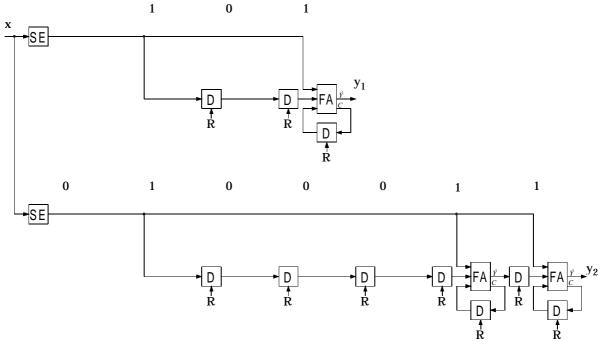
b) Sort cells by starting time and size: u₂, V₄, u₁, V₆, V₃, V₅, V₁, V₂. Allocate a cell and assign variables from the list. Remove assigned variables from the list. Allocate new cell when no variables fits.

Cell	Variables
0	u ₂ , V ₆
1	V_4
2	u ₁ , V ₃
3	V ₅
4	V ₁
5	V ₂

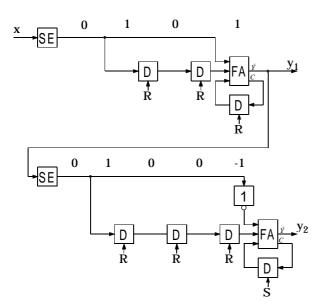




b) There is no difference in numbers of full-adders and flipflops in case of 2's complement and CSDC description of the coefficient.

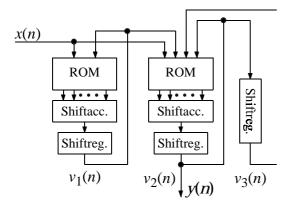


c) Reuse multiplication result y1 and multiply it with 7 implemented using CSDC (7 = $8-1 = 100-1_{CSDC}$)



5. a) Must compute inputs to delay elements and the output values.

$$\begin{split} v_1(n+1) &= x(n) + av1(n) \\ v_2(n+1) &= y(n) \\ y(n) &= x(n) + av1(n) + bv1(n) + cv2(n) + dv3(n) \\ &= x(n) + (a+b)v1(n) + cv2(n) + dv3(n) \end{split}$$



b) Problem with the calculation of y(n). Split this into two subcalculations by pipelining between the two additions. Call the added delay element $v_4(n)$

