Solutions to exam 2019-01-07 in TSTE86 Digital ICs

1.

a) $S_n = (A+B)CD \Rightarrow F = \overline{S_n(A,B,C,D)} = \overline{(A+B)CD}$

b) $S_p = AB + C + D \Rightarrow F = S_p(\bar{A},\bar{B},\bar{C},\bar{D}) = \bar{A}\bar{B} + \bar{C} + \bar{D} = \overline{(A+B)CD}$
$\overline{S_n(A,B,C,D)} = S_p(\bar{A},\bar{B},\bar{C},\bar{D})$ shows that the nets are complementary

c) Design all PMOSFETs in a single branch to have equal *R* as inverter PMOS:

$R_{\text{on}} \propto \frac{1}{W}$, let $W_{P,A} = W_{P,B} \Rightarrow$

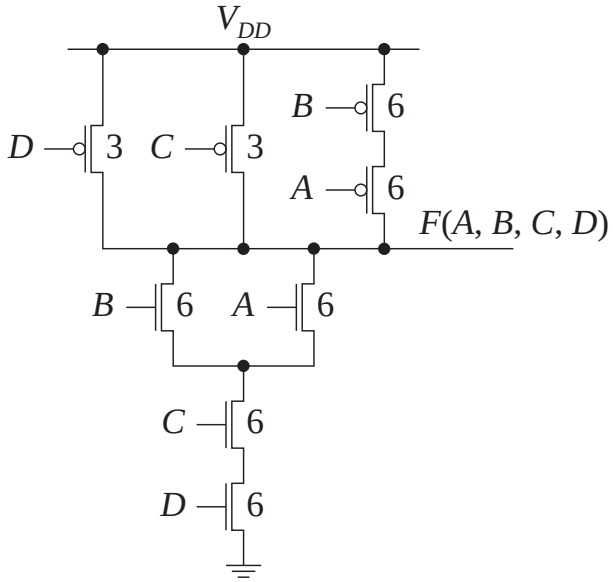
$\frac{1}{W_{P,A}} + \frac{1}{W_{P,B}} = \frac{2}{W_{P,A}} = \frac{2}{W_{P,B}} = \frac{1}{W_{P,C}} = \frac{1}{W_{P,D}} = \frac{1}{3L} \Rightarrow \begin{cases} W_{P,A} = W_{P,B} = 6L \\ W_{P,C} = W_{P,D} = 3L \end{cases}$

Design all NMOSFETs in a single branch to have equal *R* as inverter NMOS:

$$\left.\begin{array}{l} W_{N,A} = W_{N,C} = W_{N,D} \Rightarrow \frac{1}{W_{N,A}} + \frac{1}{W_{N,C}} + \frac{1}{W_{N,D}} = \frac{3}{W_{N,A}} = \frac{3}{W_{N,C}} = \frac{3}{W_{N,D}} = \frac{1}{2L} \\ W_{N,B} = W_{N,C} = W_{N,D} \Rightarrow \frac{1}{W_{N,B}} + \frac{1}{W_{N,C}} + \frac{1}{W_{N,D}} = \frac{3}{W_{N,B}} = \frac{3}{W_{N,C}} = \frac{3}{W_{N,D}} = \frac{1}{2L} \end{array}\right\} \Rightarrow$$

$W_{N,A} = W_{N,B} = W_{N,C} = W_{N,D} = 6L$

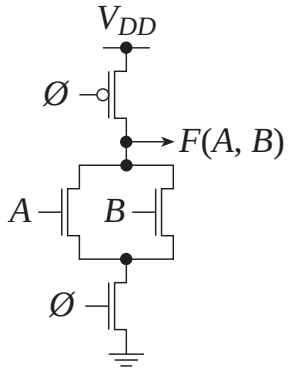
The gate with sizes indicated is shown below



d) Worst pull-up input patterns occur when a single PMOS path conducts, given by
$F(A,B,C,D) = F(1,1,1,0)$ or $F(1,1,0,1)$ or $F(0,0,1,1)$
Worst pull-down input patterns occur when a single NMOS path conducts, given by
$F(A,B,C,D) = F(1,0,1,1)$ or $F(0,1,1,1)$
Best pull-up input pattern occur when all PMOSFETs conduct, given by
$F(A,B,C,D) = F(0,0,0,0)$
Best pull-down input pattern occur when all NMOSFETs conduct, given by
$F(A,B,C,D) = F(1,1,1,1)$

2.

a) $F(A,B) = \overline{(A+B)} \Rightarrow S_n = A + B$. The transistor schematic is drawn below.

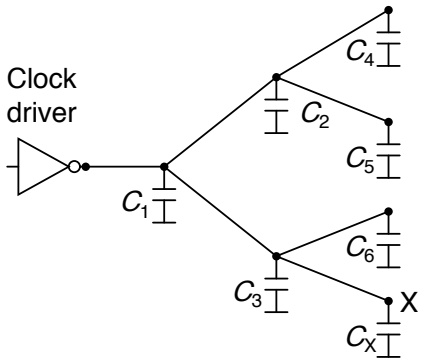


b) Node $F(A, B)$ is first precharged to V_{DD}, which is done by setting clock Ø low. Then the evaluation starts by setting clock Ø high, where a low A and low B disconnects the output from the supply, causing $F(A, B)$ to remain at V_{DD} due to the precharge. If instead either A or B are high, the output is discharged and becomes low.

c) If the circuit evaluates F to 1 and the circuit is not clocked for some time, the output voltage becomes corrupted since the charge leaks through the channels and drain junctions of the adjacent transistors. Depending on the size of leakage, there will be a minimum operation frequency that the circuit has to be clocked at to avoid corruption.

3.

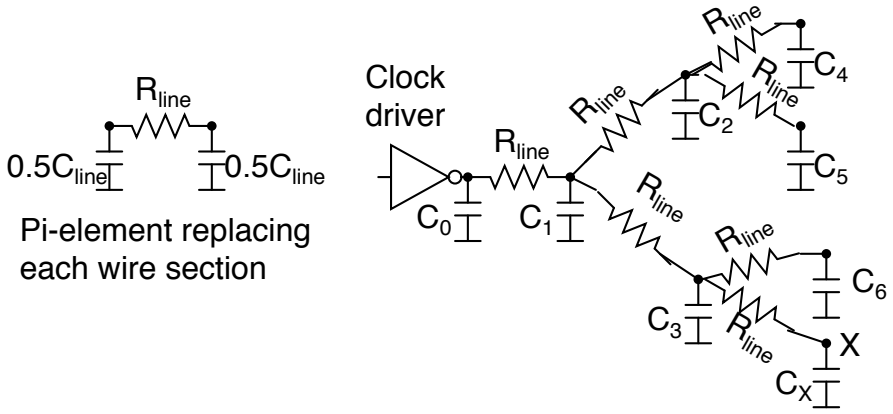
a) Each 5 mm line segment has the capacitance $C_{\text{line}} = WLC_p + 2LC_f = 1860$ fF
If R and L is neglected, parallel connection of all capacitors yields the total C



$C_1 = C_2 = C_3 = C_{\text{line}} = 1.86$ pF
$C_4 = C_5 = C_6 = C_X = C_{\text{line}} + C_L = 1.96$ pF
$C_{\text{total}} = 3C_{\text{line}} + 4(C_{\text{line}} + C_L) = 13.42$ pF

Average current is $I_{avg} = \frac{\Delta Q}{\Delta t} = \frac{C_{\text{total}} V_{\text{swing}}}{\Delta t} \approx 27$ mA

b) Replace each wire segment by a π net

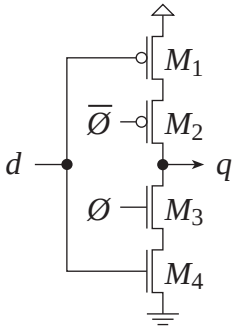


$R_{\text{line}} = R_{\text{sq}} \frac{L}{W} \approx 167\ \Omega$
$C_0 = 0.5\,C_{\text{line}} = 0.93$ pF
$C_1 = C_2 = C_3 = 1.5\,C_{\text{line}} = 2.79$ pF
$C_4 = C_5 = C_6 = C_{\text{X}} = 0.5\,C_{\text{line}} + C_{\text{L}} = 1.03$ pF

c) Use the Elmore delay formula to find the dominant time constant in node X

$\tau_{\text{X}} = R_{\text{line}}(C_1 + C_2 + C_4 + C_5) + 2R_{\text{line}}(C_3 + C_6) + 3R_{\text{line}}C_{\text{X}} = 3.06$ ns

4. The transistor schematic of a C^{2}MOS latch is shown below. When the enable signal *Ø* is high, MOSFETs M_2 and M_3 conduct, and M_1 and M_4 operates like a CMOS inverter, propagating the inverted *d* to the output *q*. When *Ø* is low, M_2 and M_3 are cut-off. Hence, *q* is isolated from the circuit and the parasitic capacitance in the node is used to store the previous output.



5. a) Multiplication algorithm $Z = X \cdot Y$

					y_3	y_2	y_1	y_0
				$\times$	x_3	x_2	x_1	x_0
				1	x_0y_3	x_0y_2	x_0y_1	x_0y_0
				$\overline{x_1y_3}$	x_1y_2	x_1y_1	x_1y_0	
			$\overline{x_2y_3}$	x_2y_2	x_2y_1	x_2y_0		
+	1	x_3y_3	$\overline{x_3y_2}$	$\overline{x_3y_1}$	$\overline{x_3y_0}$			
	z_7	z_6	z_5	z_4	z_3	z_2	z_1	z_0

Partial products in squaring 1001_{2C} and output 00110001_{2C}

					1	0	0	1
				$\times$	1	0	0	1
				1	0	0	0	1
				1	0	0	0	
			1	0	0	0		
+	1	1	1	1	0			
~~1~~	0	0	1	1	0	0	0	1

b) There are several critical paths with a propagation delay of one AND gate and nine FAs $\Rightarrow t_d = 1t_{AND} + 8t_{FA} = 1 \cdot 0.3 + 9 \cdot 0.7$ ns = 6.6 ns

c) Full adders with a zero in computing z_1, z_2, and z_3 can be simplified to half adders, the full adder with a one in can be simplified to a half adder with inverted inputs and outputs, and the full adder that computes z_7 can be simplified to an XOR gate.

6. a) *Observability* is a property that measures the ease of observing the state of an internal circuit node at the circuit output. *Controllability* is a property that measures the ease of setting the state of an internal circuit node from the circuit input. An *ad-hoc test* is a collection of tricks and techniques that aims at increasing the observability and controllability, often tailored to a particular application

b) $m = 0$ for the Sa0 fault
To obtain $m = 1$ we need $ab \neq 11$
To propagate $m = 1$ to the z we need $n = 1$ and $p = 1$, obtained by $ac \neq 11$ and $bc \neq 11$
Jointly $abc \neq$ 11-/1-1/-11
Possible test patterns for $z = 1$ are abc = 000/001/010/100
The Sa0 fault for node m is detected by observing $z = 0$ for one of those patterns