4) Multipliers are important design blocks in many integrated circuit designs. Fig. 2 shows the block diagram of a basic 4-by-4-bit array multiplier, where FA and HA are full-adders and half-adders, respectively. For an array multiplier, the critical path delay when multiplying two binary words that are M and N bits wide is

$$t_{mult} = [(M–1)+(N–2)]t_{carry} + (N–1)t_{sum} + t_{and}$$

where

t_{carry} = input-to-output carry propagation delay,
t_{sum} = delay between input carry and sum bit, and
t_{and} = AND-gate propagation delay.

a) Modify the array multiplier structure so that it becomes a 4-by-4-bit carry-save multiplier. Draw the block diagram for the carry-save multiplier. (2 p)

b) Derive an expression for the critical path delay in the carry-save multiplier. Clearly mark the critical path in the block diagram. (1 p)

c) What are the advantages and disadvantages with the carry-save multiplier compared to the array multiplier regarding critical path and circuit area? (1 p)

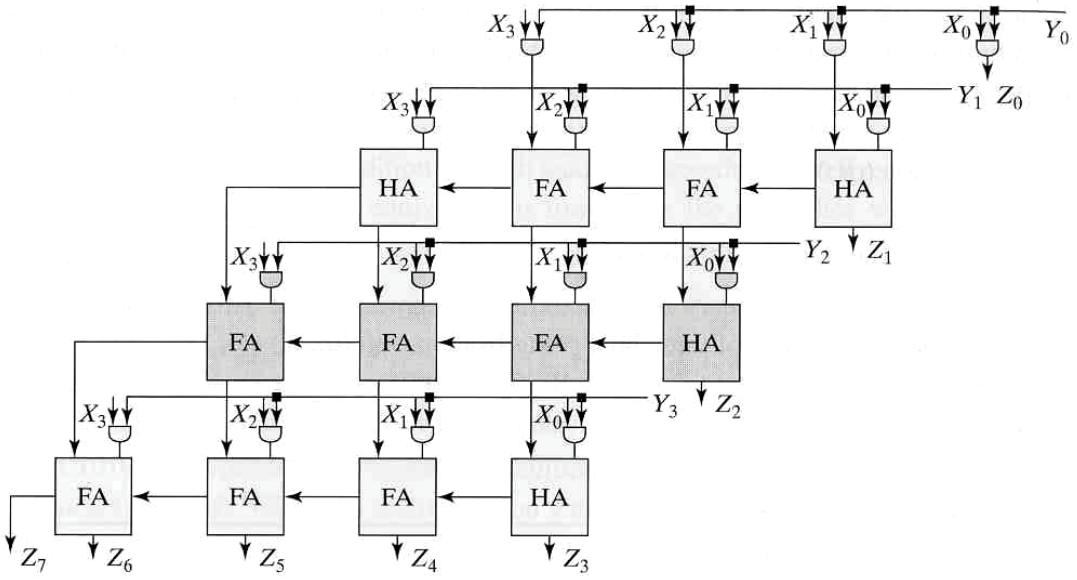

Fig. 2. Array multiplier block diagram.

4 a) In a carry-save multiplier, carry-bits are not immediately added, but are rather "saved" for the next adder stage. In the final stage, carries and sums are merged in a fast carry-propagate adder stage (vector-merging adder). The carry-save multiplier structure is shown in the figure below.

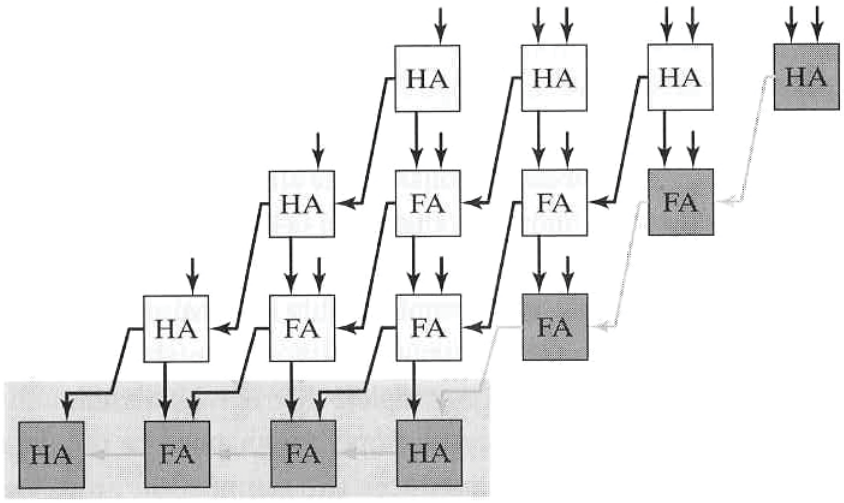

Fig. 1. Carry-save multiplier

b) The critical path delay for a carry-save multiplier is

$$t_{mult} = [M + (N–1)]t_{carry} + t_{and}$$

c) To determine the critical path for an array multiplier is not so straightforward. A large number of paths of almost identical length can be identified. The advantage of a carry-save multiplier is that the critical path is shorter and uniquely defined compared to an array multiplier. A disadvantage is the slight area increase due to the vector merging adder.