Solutions to exam 2018-08-31 in TSTE85 Low Power Electronics

1.

a) Wrist watches, pocket calculators, cellular phones, pagers, hearing aids, pacemakers.

b) The principle of clock gating is to turn off the clock signal in parts of the digital circuit while is not needed for computations. This is done by connecting the clock signal to a gate where control signals determines if the clock should be on or off in the particular circuit. This technique lowers the dynamic power consumption due to lower switching activity of the clock input transistors and it also can prevent circuits to do unnecessary calculations.

c) When the PLL is duty cycled, the control loop is opened when no data is transmitted and closed just before transmission. Hence the circuits in the loop can be put into a sleep mode when there is no transmission, leaving only the oscillator on that otherwise would incur a long start up penalty time.

d) Main advantage is that an asynchronous circuit can be designed for average delay performance, which is a great benefit in subthreshold mode where the uncertainty in timing is large. This is in contrast with synchronous logic that has to be designed for worst-case delay performance. The combination of asynchronous and subthreshold should also give a very low EMI.

e) If an input switches while the power clock is high, it corresponds to a standard switching in static CMOS logic, yielding an increased voltage drop over the transistors and corresponding increase in energy dissipation.

2.

a) $I_D = 0.5\cdot 10^{-6} e^{-25|V_{GTn}|} = ke^{-|V_{GT}|/(n_s V_\Theta)} \Rightarrow n_s V_\Theta = 25^{-1} \Rightarrow S = n_s V_\Theta \ln(10) \approx 92$ mV/decade

b) $P_{\text{rel}} = 1 - \frac{I_{D1}V_{DD}}{I_{D0}V_{DD}} = 1 - \frac{ke^{-25|V_{GT1}|}V_{DD}}{ke^{-25|V_{GT0}|}V_{DD}} = 1 - e^{25(|V_{GT0}|-|V_{GT1}|)} = 1 - e^{25(|-0.3|-|-0.4|)} \Rightarrow 1 - e^{-2.5} \approx 92\%$

c) For example, decreasing the bulk potential of the NMOSFET would increase V_{SBn}, which increases V_{Tn}.

3. n-bit Gray counter: Designed for 1 transition/state for the entire word.
n-bit binary counter: The LSB make 1 transition/state.
The bit on the next, higher significant level has a halved transisition activity, etc ⇒
$\sum_{i=0}^{n-1} 2^{-j} = 2 - 2^{1-n} \to 2$ transitions/count for large n, which yields the relative figure of two times more transitions for the binary counter than the Gray counter.

4.

a) One's probability for $P(f_j)$

$$P\left(\overline{a_j}\right)P\left(b_j\right)P\left(c_j\right)+P\left(a_j\right)P\left(\overline{b_j}\right)P\left(c_j\right)+P\left(a_j\right)P\left(b_j\right)P\left(\overline{c_j}\right)+P\left(a_j\right)P\left(b_j\right)P\left(c_j\right)=$$

$$=\frac{1}{2}\cdot\frac{1}{2}\cdot\frac{1}{4}+\frac{1}{2}\cdot\frac{1}{2}\cdot\frac{1}{4}+\frac{1}{2}\cdot\frac{1}{2}\cdot\frac{3}{4}+\frac{1}{2}\cdot\frac{1}{2}\cdot\frac{1}{4}=\frac{3}{8}$$

Determine transition activities

$\alpha_a = \alpha_{a01} + \alpha_{a10} = 2P(a_j)[1–P(a_j)] = 1/2$

$\alpha_b = 1/2$

$\alpha_c = 2\cdot(1/4)\cdot(1–1/4) = 3/8$

$\alpha_f = \alpha_{f01} + \alpha_{f10} = 2P(f_j)[1–P(f_j)] = 2(3/8)[1–3/8] = 15/32$

Determine the switch activity

$a = \sum(\alpha_{i01}C_i)/\sum C_i = (1/64)[(16C_a+16C_b+12C_c+15C_f)/(C_a+C_b+C_c+C_f)]$

Determine the switched capacitance

$C_{sw} = a\sum C_i = (1/64)(16C_a+16C_b+12C_c+15C_f) = aC_{tot}$

The power consumption is given by

$P = afC_{tot}V_{DD}^2 = fV_{DD}^2(1/64)(16C_a+16C_b+12C_c+15C_f)$

b) The power reduction is

$1 – a(0.8f)C_{tot}(0.85V_{DD})^2/(afC_{tot}V_{DD}^2) = 0.422 \approx 42\%$

5.

a) Thermal noise.

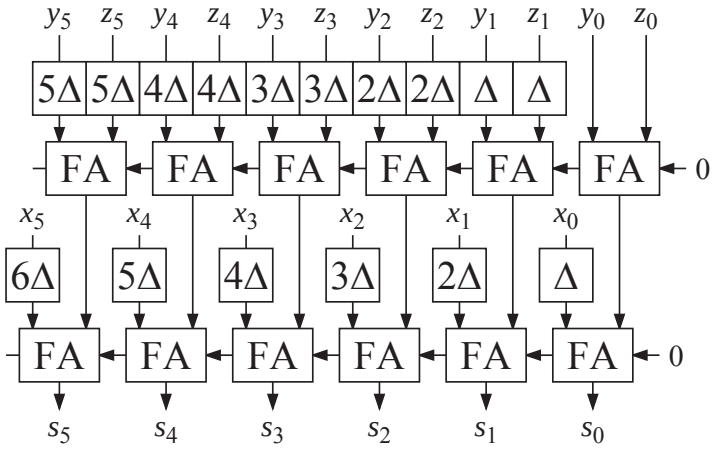
b) Circuit gain must be larger than one.

c) SNR $\approx 6n + 1.8 \Rightarrow n \approx$ (SNR – 1.8)/6
According to the graph, digital power is less than analog for approximately
SNR $\geq$ 31 dB $\Rightarrow n \geq 4.9 \approx 5$ bits

6.

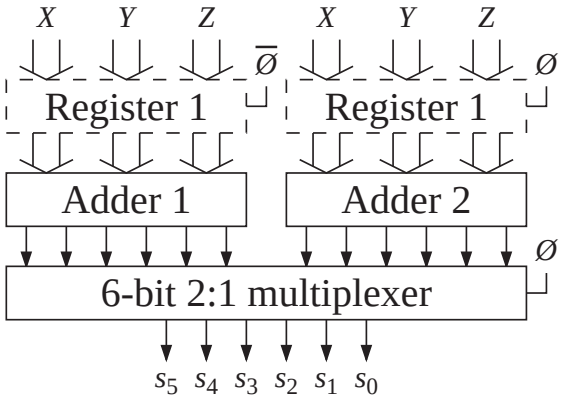
a) When the inputs switch at different times, the FA will operate on the wrong input during the time difference. This could potentially cause a glitch with extra energy consumption $E_g = CV_gV_{DD}$, where V_g is the amplitude of the glitch.

b) A delay balanced adder where Δ can be implemented with two cascaded inverters is shown below



The power dissipation of a basic circuit increases as $P(\tau) = P \cdot 2^{\tau/k}$, where τ is the skew. Since $\tau = 100$ ps $\Rightarrow \tau/k = 1$, $k = 100$ ps. Assume P consumption of inverter is P_0. The original adder have 12 FAs with skews {0,1,1,2,2,3,3,4,4,5,5,6} times 60 ps, yielding the power dissipation $P_{\text{old}} = 5P_0(1 \cdot 2^0 + 2 \cdot 2^{0.6} + 2 \cdot 2^{1.2} + 2 \cdot 2^{1.8} + 2 \cdot 2^{2.4} + 2 \cdot 2^{3.0} + 2^{3.6}) = 271.36P_0$. In the delay balanced adder, all skews are zero, yielding a power dissipation for the FAs that is $P_{\text{add}} = 12 \cdot 5P_0 = 60P_0$. However, the additional delay of 3(1+2+3+4+5)+6 times 60 ps requires 2[3(1+2+3+4+5)+6] = 102 inverters drawing the power $P_\Delta = 102P_0$. Total power becomes $P_{\text{new}} = 162P_0$.
Power saving is $1 - P_{new}/P_{\text{old}} \approx 0.40 = 40\%$.

c) An interleaved adder is shown below



Neglecting registers, critical path is $t_c = 7t_{\text{FA}} = 7 \cdot 60$ ps = 420 ps. Since the interleaved adder should obtain twice the throughput, the supply voltage can be scaled until $t_{\text{new}} = 2t_{\text{c}} - t_{\text{mux}} = 2 \cdot 420 - 50$ ps = 790 ps for maintained throughput. Omitting imaginary roots, we obtain

$$\frac{t_{new}}{t_{old}} = \frac{790}{420} = \frac{V_{new}}{\left(V_{new} - V_t\right)^{1.5}} \frac{\left(V_{old} - V_t\right)^{1.5}}{V_{old}} = \frac{V_{new}}{\left(V_{new} - 0.25\right)^{1.5}} \frac{\left(1.0 - 0.25\right)^{1.5}}{1.0} \Rightarrow V_{new} \approx 0.60 \text{ V}$$

Approximately twice the C is switched at double f, yielding P savings

$$1 - \frac{\left(f/2\right)2CV_{new}^2}{fCV_{old}^2} \approx 0.64 = 64\%$$

7.

a) $f_{\overline{c2}} = a_2\overline{b_2} + 0\left(a_2 + \overline{b_2}\right) = a_2\overline{b_2}$

$f_{c2} = a_2\overline{b_2} + 1\left(a_2 + \overline{b_2}\right) = a_2 + \overline{b_2}$

$\text{ODC}_{c2} = f_{\overline{c2}} f_{c2} + \overline{f_{\overline{c2}}}\,\overline{f_{c2}} = a_2\overline{b_2}\left(a_2 + \overline{b_2}\right) + \overline{a_2\overline{b_2}}\,\overline{\left(a_2 + \overline{b_2}\right)} = a_2\overline{b_2} + \overline{a_2\overline{b_2} + \left(a_2 + \overline{b_2}\right)} =$

$= a_2\overline{b_2} + \overline{a_2 + \overline{b_2}} = a_2\overline{b_2} + \overline{a_2}b_2 = a_2 \oplus b_2$

b) A realization of the subset-disabling precomputed comparator is shown below