# Solutions to exam 2018-04-05 in TSTE85 Low Power Electronics

1.

a) Average power determines battery life time and cooling requirements. Peak power determines the width of power supply wires, number of bonding wires, and amount of bypass capacitors, and affects the design effort required for proper signal integrity.

b) The dynamic power dissipation is input-pattern dependent, and the inputs may not be known beforehand.

c) Bandwidth and required signal-to-noise ratio of the analog signal.

d) It has more power consuming stages than a homodyne (zero IF) transceiver or a transceiver that processes the signals with low IF.

e) If an input switches while the power clock is high, it corresponds to a standard switching in static CMOS logic, yielding an increased voltage drop over the transistors, and hence the energy dissipation increases.

f) The average power consumption of wireless systems is mainly determined by the *power management* and *communication protocols*.

2. Wireless sensor with energy density $D$ = 2.4 J/mm$^3$, average power $P_{sensor}$ = 0.15 mW, operation time $t_{use} \approx 365 \cdot 24 \cdot 60 \cdot 60$ s = 31.5 Ms.

a) Battery volume with efficiency $\eta_b = 0.90$

$$V_{battery} = \frac{P_{sensor} t_{use}}{\eta_b D} \approx 2.2 \text{ cm}^3$$

b) Charge efficiency is $\eta_s = 0.80$

Average charge power needed from solar cell is $P_{charge} = P_{sensor}/\eta_b/\eta_s \approx 0.21$ mW

Number of hours in a month is $N \approx 24 \cdot 31$ h = 744 h

Average power per area supplied in worst-case month $P_{area} = 70 \cdot 30/744$ W/m$^2$

Solar cell area needed to charge battery

$$A = \frac{P_{charge}}{P_{area}} \approx \frac{0.21 \cdot 10^{-3} \cdot 744}{70 \cdot 30} \text{ m}^2 \approx 7.4 \cdot 10^{-5} \text{ m}^2 = 0.74 \text{ cm}^2$$

A thickness of 0.2 mm yields a solar cell volume of about 15 mm$^3$

c) Relying on an average distribution of sun per month, the battery needs to last 1/12th of a year. Hence the volume is $V_{both} = V_{battery} / 12 \approx 180$ mm$^3$. (A worst-case assumption of sun in beginning and end of subsequent two months would require almost double size)

3.

a) Bundled data design.

b) The timing signal should arrive to the register with a delay such that the entire bundle of data has been calculated and received by the register.

c) Asynchronous design generates less current peaks, lower electromagnetic emission, and may have an increased power efficiency compared with clocked Boolean logic. However, the asynchronous design have a more varying performance with operation conditions, and its operation will break if the timing signals are not designed conservatively enough. This especially noticeable for subthreshold current designs, for which there are exponentially variations in subthreshold current with process, voltage, and temperature variations.

d) Data bits are encoded with null states, which enable the delay blocks to be replaced with Completion detection blocks generating the Acknowledge signals. By this the circuit will continue working in the presence of operation conditions, resulting in an average case performance behavior instead of potential failure.

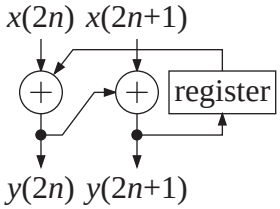
4.

a) The load of the clock MOSFETs is $2C_g$, yielding $P_{d,clk} = 2C_g f_{clk} V_{DD}^2$.

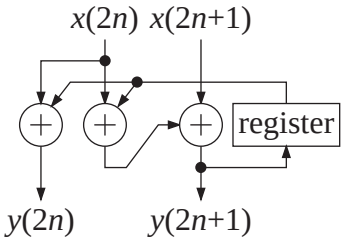
b) Due to the precharge, there is a transition $0 \rightarrow 1$ on $F$ when $F$ is evaluated to 0, but no transition when $F$ is 1. Hence $\alpha_{01} = P(X=0) = 1-P_X$. The dynamic power dissipation becomes $P_d = (1-P_X)C_l f_{clk} V_{DD}^2$.

5.

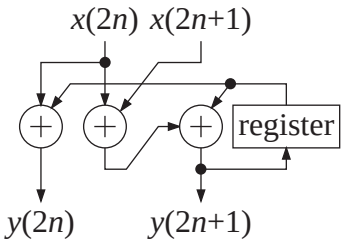
a) Signal-flow graph after loop unrolling:




b) To improve the latency of the critical loop, we need to transform operations out of the loop by reordering the additions. Start by simplifying the critical loop by moving the addition $x(2n) = x(2n) + y(2n)$ out of the loop. It can made by duplicating the left-most addition in b) according to the figure below.

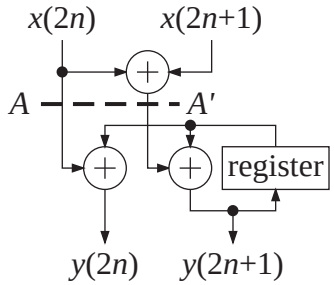



Reorder the additions such that the loop is shortened to one adder and one register. This is made in the figure below by swapping the order of adding $x(2n+1)$ and the register output.




This signal-flow graph has a critical loop with only one adder and one register and does hence solve our problem.

c) The critical path of the algorithm in b) (redrawn below) goes through one register and two adders. This path can be reduced to one register and one adder by introducing pipelining in the sequential parts of the algorithm, obtaining the same latency of the critical path as that of the loop. A cut A—A' suitable for inserting two pipeline registers to accomplish this is indicated in the figure below.




d) Assume the energy consumption of a register operation to be $E_{reg}$ and of an addition operation $E_{add}$. To perform an accumulation operation the algorithm in c) consumes the energy $E_d = N/2(3E_{reg}+3E_{add}) = 1.5N(E_{reg}+E_{add})$ while the original algorithm consumes $E_0 = N(E_{reg}+E_{add})$. Hence the algorithm in c) consumes 50% more energy if the same supply voltage is used.

e) The period for completing an accumulation operation with the algorithm in c) is $T_1 = 0.5NkV_{DD1}(V_{DD1}-V_T)^{-1.5}$, where $k$ is a proportionality constant, while the original algorithm yields the period $T_0 = NkV_{DD0}(V_{DD0}-V_T)^{-1.5}$. With the same throughput requirement,

$$T_1 = T_0 \Rightarrow \frac{V_{DD1}}{2\left(V_{DD1}-V_T\right)^{1.5}} = \frac{V_{DD0}}{\left(V_{DD0}-V_T\right)^{1.5}}.$$

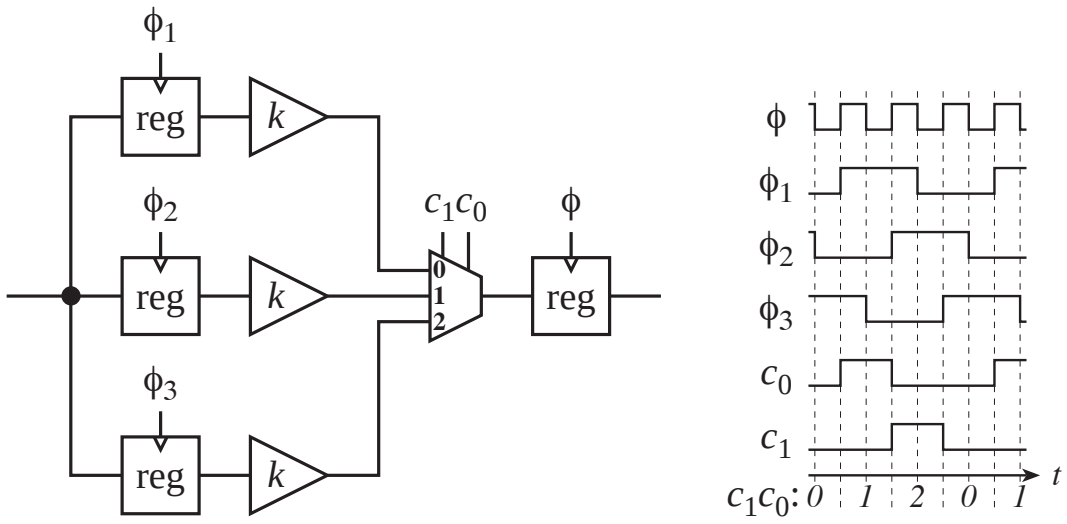
Solving this equation numerically, we obtain $V_{DD1} \approx 0.93$ V.
Assuming the load capacitances of a register and an adder are $C_{reg}$ and $C_{add}$, respectively, we obtain the relative energy consumption

$$\frac{E_1}{E_0} = \frac{\frac{N}{2}3\left(E_{reg}+E_{add}\right)\Big|_{V_{DD}=V_{DD1}}}{N\left(E_{reg}+E_{add}\right)\Big|_{V_{DD}=V_{DD0}}} = \frac{3}{2}\frac{\left(C_{reg}+C_{add}\right)V_{DD1}^2}{\left(C_{reg}+C_{add}\right)V_{DD0}^2} = \frac{3}{2}\frac{V_{DD1}^2}{V_{DD0}^2}$$

Numerically $E_1/E_0 \approx 0.58$. Hence the energy savings becomes approximately 42%.

6.

a) Multiplier interleaved with a factor of three and its timing




b) The propagation delay of the original circuit is 0.5 ns according to Figure 5.

The throughput of the original circuit is $B = 2 \cdot \frac{1}{0.5 \cdot 10^{-9}}$ samples/s = 4 Gsamples/s

To maintain the same throughput of the new circuit, $t_p$ is selected as

$$B = 2 \cdot \frac{1}{0.5 \cdot 10^{-9}} = 3 \cdot \frac{1}{t_p} \Rightarrow t_p = \frac{3}{2} \cdot 0.5 \cdot 10^{-9} \text{ ns} = 0.75 \text{ ns}$$

The minimal supply voltage of the new circuit is then ~1.5 V according to Figure 5. The power saving becomes

$$1 - \frac{P_1}{P_0} = 1 - \frac{f_1 C_1 V_1^2}{f_0 C_0 V_0^2} = 1 - \frac{\frac{2}{3} f_0 \cdot \frac{3}{2} C_0 \cdot 1.5^2}{f_0 \cdot C_0 \cdot 2.4^2} \approx 0.61 = 61\%$$