Linköping Institute of Technology
Department of Electrical Engineering, Integrated Circuits and Systems

Exam TEN1 in TSTE85 Low Power Electronics

Time:	Monday 13 January 2020, 8:00–12:00
Place:	TER4
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aid:	Calculator
Maximum score:	70 points
Grades:	50 points for 5 40 points for 4 30 points for 3
Solutions:	Posted on the course web
Result:	Posted through LADOK by 29 January 2020

1. Explain what a static leakage current in a CMOS circuit is and give two examples of how static leakage currents can be reduced. (4 p)

2. Consider an ideal three-input NAND gate with independent and uniformly random inputs (a, b, c). What input probabilities $P(a=1)=P(b=1)=P(c=1)$ would cause the highest transition activity at the output? Motivate your answer. (6 p)

3. Lithium-ion batteries are popular in mobile equipment as the energy density is high. In the table in Figure 1 to the right, average voltage and specific capacity are shown for different lithium-ion battery technologies.

Material	Voltage	Capacity
$LiCoO_2$	3.7 V	140 mAh/g
$LiMn_2O_4$	4.0 V	100 mAh/g
$LiNiO_2$	3.5 V	180 mAh/g
$LiFePO_4$	3.3 V	150 mAh/g

Figure 1. Voltage and specific capacity for different battery technologies.

   a) Order the battery technologies with respect to energy density. (4 p)

   b) A laptop battery with an average voltage of at least 16 V should be designed. The battery should last for approximately 4 h with an average power consumption of 15 W. Calculate the weights of a battery based on the different technologies above. (4 p)

4. A digital CMOS circuit is overdesigned a factor R in clock frequency. How much power can be saved utilizing supply voltage scaling? Assume that the propagation delay is proportional to $V_{DD}/(V_{DD}-V_T)$, R is 1.5, and original supply voltage is V_{DD} = 1.5 V.

   a) Solve the problem assuming V_T = 0.40 V. (5 p)

   b) Solve the problem assuming V_T = 0.30 V. (5 p)

5. The circuit in Figure 1 realizes the function $f = a \oplus b \oplus c$ with two XOR gates.

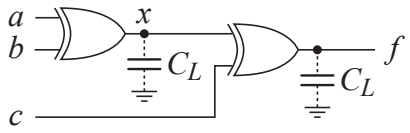

Figure 1. Two cascaded XOR gates.

   a) The propagation time t_d (the time required to drive the output voltage from V_{DD} to $V_{DD}/2$ or from ground to $V_{DD}/2$) for the XOR gates in Figure 1 is 1 ns. Sketch the voltages in node f and x as functions of time when the inputs <a,b,c> changes from <0,0,0> to <0,1,1>. Consider a, b, and c as ideal. (3 p)

   b) Calculate the dissipated energy due to the two capacitances C_L. (3 p)

   c) A delay of 1 ns is introduced for signal c relative to a and b. Sketch the output voltage and calculate the dissipated energy. (4 p)

6. Consider a stepwise charging of a capacitive load that is initially discharged. Two power supply voltages, V_{DD1} and V_{DD2}, are used.

a) Derive the dissipated energy when $V_{DD1} < V_{DD2}$ and the steps are long in time. (6 p)

b) Derive the optimal ratio between V_{DD1} and V_{DD2} in order to obtain minimal energy dissipation. (6 p)

7. The datapath shown in Figure 3 should operate at a frequency of 125 MHz. The critical path is indicated for each component assuming a nominal power supply voltage of 1.5 V. Assume that a block consumes power P_0 at nominal supply voltage, $V_T = 0.33$ V, and $r = 2$.

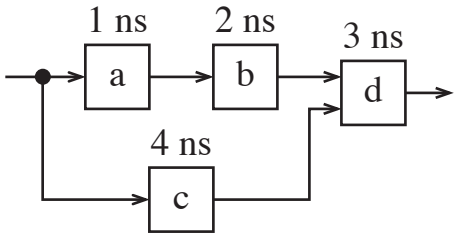

Figure 2. Datapath.

a) Perform power supply voltage scaling of the system and compute the power saving relative the data path operating at nominal power supply voltage. (6 p)

b) Introduce one level of pipelining in the system and compute the power savings. Neglect power and delay of registers. (4 p)

8. A low power wireless system should be active for 1 ms and then go to sleep for 999 ms before repeating the cycle. The transceiver consumes 2 mW in active mode and 200 nW in sleep mode. A sleep timer that consumes the power 10 nW with accuracy 500 ppm is used to control the sleep (1 ppm = 0.0001%).

a) Calculate the power consumption of the system if we allow it to skip transmission events due to late wake up. (3 p)

b) Calculate the power consumption of the system if we do <u>not</u> allow it to wake up late. (4 p)

c) Assume that we redesign the system to use a sleep timer with power 40 nW and accuracy 200 ppm. Recalculate the power consumption of the system if we do <u>not</u> allow it to wake up late. (3 p)

TSTE85 FORMULAS

Circuits

Transition activity $\alpha = \alpha_{01} + \alpha_{10} = 2\alpha_{01} = 2\alpha_{10}$

Switch activity $a = \sum_i \alpha_{01,i} C_i \Big/ \sum_i C_i$

Switched capacitance $C_{sw} = a \sum_i C_i$

Dynamic power consumption $P_d = f_{clk} C_{sw} V_{pp} V_{DD}$

Short-circuit power consumption $P_{sc} = a f_{clk} t_{sc} I_{peak} V_{DD}$

Propagation time $t_p \propto V_{DD} \Big/ \left(V_{DD} - V_T\right)^r$, $1 \le r \le 2$

MOSFETs

Threshold voltage $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$

Weak inversion ($V_{GT} < 0$) $I_D = I_{D0}\left(W/L\right) e^{-\left|V_{GT}\right|/\left(n_s V_\Theta\right)} \left(1 + \lambda V_{DS}\right)$

where

$V_\Theta \approx 26$ mV @ $T = 300$ K

n_s can be calculated from $S = n_s V_\Theta \ln(10)$

Strong inversion ($V_{GT} \ge 0$) $I_D = k'\left(W/L\right) V_{min} \left(\left|V_{GT}\right| - V_{min}/2\right)\left(1 + \lambda V_{DS}\right)$

where

$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$ (corresponding to *saturation*, *resistive*, and *velocity saturation* modes)

Gate-oxide leakage $I_G = k_1 W \left(V_{ox}/t_{ox}\right)^2 e^{-k_2 t_{ox}/V_{ox}}$

Logic

Shannon's expansion theorem $\overline{f\left(x, y, z, \ldots, +, \cdot\right)} = f\left(\bar{x}, \bar{y}, \bar{z}, \ldots, \cdot, +\right)$

Cofactors $f_{\bar{x}} = f\left(x, y, z, \ldots\right)\Big|_{x=0}$, $f_x = f\left(x, y, z, \ldots\right)\Big|_{x=1}$

Expansion in sum and product $f\left(x, y, z, \ldots\right) = \bar{x} \cdot f_{\bar{x}} + x \cdot f_x = \left(x + f_{\bar{x}}\right)\left(\bar{x} + f_x\right)$

Observability Don't Care set $\mathrm{ODC}_x = f_{\bar{x}} f_x + \overline{f_{\bar{x}}}\,\overline{f_x}$