Linköping Institute of Technology
Department of Electrical Engineering, Integrated Circuits and Systems

Exam TEN1 in TSTE85 Low Power Electronics

Time:	Friday 11 January 2019, 8:00–12:00
Place:	G34
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aids:	Calculator and appended formula page
Maximum score:	70 points
Grades:	50 points for 5 40 points for 4 30 points for 3
Solutions:	Posted on the course web
Results:	Posted through LADOK by Tuesday 29 January 2019

1.

a) Give examples on historical applications that have been driving forces in the field of low power electronics. (3 p)

b) Describe how the following software strategies can be used to obtain a low power system: *transition strategies, load-change strategies, adaptation strategies*. (3 p)

c) Describe the impact of average and peak power consumption on a chip design. (2 p)

d) Why is it more power efficient to use an on-chip inductor compared with an external inductor? (2 p)

e) Explain how precomputation of a logic function can be used to reduce the power consumption. (2 p)

2. Explain what a static leakage current in a CMOS circuit is and give two examples of how static leakage currents can be reduced. (4 p)

3. In Figure 1 a static CMOS inverter is driving an identical inverter and an interconnect. The interconnect is assumed to be short in length and is modeled as a lumped capacitor. The parasitic capacitances in the two inverters are dominated by the transistor capacitances. The input capacitance of the inverter is C_{in}, the output capacitance is C_{out}, and the interconnect capacitance is C_w. The power supply voltage is V_{DD} = 1.2 V and the threshold voltage for the transistors is $|V_T|$ = 0.4 V. Assume $C_{in} = C_{out} = C_0$, $C_w = 4C_0$. Neglect channel length modulation in calculation of MOSFET currents ($\lambda \approx 0$).

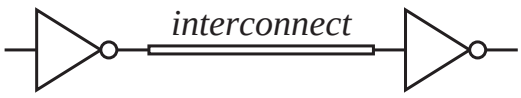

Figure 1. Inverter loaded with interconnect and an identical inverter.

a) Estimate the relative change in dynamic power consumption when the transistor widths are increased to double the original size, and voltage scaling is used to maintain the total propagation delay from the input of the first inverter to the input of the second inverter. Assume long transistor channels with saturated MOSFETs during charge. (5 p)

b) Estimate the relative change in dynamic power consumption when the transistor widths are increased to double the original size, and voltage scaling is used to maintain the total propagation delay from the input of the first inverter to the input of the second inverter. Assume short transistor channels with r = 1.5 during charge. (5 p)

4. The capacitor C is charged in sequence by two power supplies as shown in Figure 2. At time t_0 the first power supply with supply voltage V_{DD}/X is connected. When the voltage V over C has settled at time t_1, the first power supply is disconnected and the second power supply with supply voltage V_{DD} is connected to C. The voltage V has finally settled at time t_2.

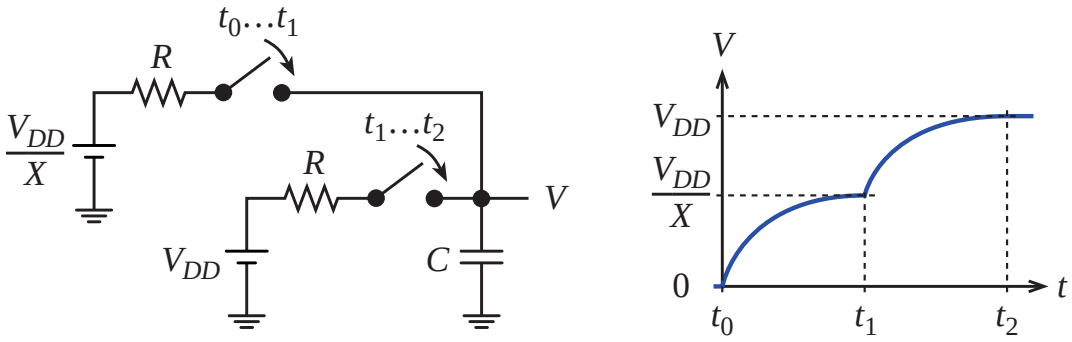

Figure 2. Stepwise charging of a capacitor.

a) How much energy is stored in the capacitor C at time t_1? (2 p)

b) How much energy is stored in the capacitor C at time t_2? (2 p)

c) How much energy has been drawn from the power supplies between time t_0 and t_2 due to the charging of C? (4 p)

d) How should the value of X be chosen to minimize the energy drawn from the power supplies as derived in c)? (4 p)

5. A logic circuit is shown in Figure 3. Determine the dynamic power consumption due to charging and discharging of the indicated capacitors in circuit nodes a, b, c, x, and F, where the unit capacitance C_0 = 5.0 fF. Assume static CMOS logic with a power supply voltage V_{DD} = 1.2 V and clock frequency f = 1 GHz. The input signals are glitch free, uncorrelated, and random with one's probabilities $P(a{=}1) = 0.1$, $P(b{=}1) = 0.2$, and $P(c{=}1) = 0.3$.

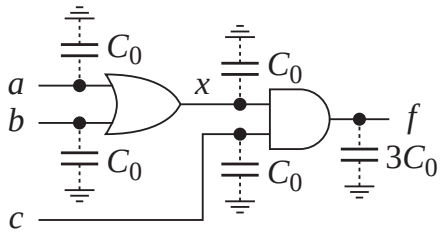

Figure 3. Logic circuit.

a) Solve the problem assuming a zero-delay model. (6 p)

b) Solve the problem assuming a unit-delay model. (6 p)

6. Consider an ideal analog integrator circuit where all current taken from the supply is used to charge the integrating capacitor at the output. The supply voltage is V_{DD} and the output capacitance is C. A sinusoidal signal with frequency f and voltage swing $V_{pp} < V_{DD}$ is output. Assume the signal-to-noise ratio to be determined by the thermal noise according to $\mathrm{SNR} = 10\log\left(CV_{pp}^2\right) - 10\log\left(8kT\right)$, where k is Boltzmann's constant and T is the absolute temperature.

   a) Derive an expression for the dissipated power. (2 p)

   b) Show that the power dissipation for the circuit is determined by the requirements on SNR, operating frequency, and temperature. (5 p)

7. Four numbers should be added with three two-input adders. The numbers are input from registers.

   a) What structure of connecting the adders is preferred from a low power point of view? Motivate your answer. (3 p)

   b) How can the power consumption be reduced using pipelining? What are the effects on the implementation? (4 p)

   c) How can the power consumption be reduced using interleaving? What are the effects on the implementation? (4 p)

   d) How is the power consumption affected if both pipelining and interleaving are applied to the circuit? (2 p)

TSTE85 FORMULAS

Circuits

Transition activity $\alpha = \alpha_{01} + \alpha_{10} = 2\alpha_{01} = 2\alpha_{10}$

Switch activity $a = \sum_i \alpha_{01,i} C_i \Big/ \sum_i C_i$

Switched capacitance $C_{sw} = a \sum_i C_i$

Dynamic power consumption $P_d = f_{clk} C_{sw} V_{pp} V_{DD}$

Short-circuit power consumption $P_{sc} = a f_{clk} t_{sc} I_{peak} V_{DD}$

Propagation time $t_p \propto V_{DD} \Big/ \left(V_{DD} - V_T\right)^r$, $1 \le r \le 2$

MOSFETs

Threshold voltage $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$

Weak inversion ($V_{GT} < 0$) $I_D = I_{D0}\left(W/L\right) e^{-\left|V_{GT}\right| / \left(n_s V_\Theta\right)} \left(1 + \lambda V_{DS}\right)$

where

$V_\Theta \approx 26$ mV @ $T = 300$ K

n_s can be calculated from $S = n_s V_\Theta \ln(10)$

Strong inversion ($V_{GT} \geq 0$) $I_D = k'\left(W/L\right) V_{min} \left(\left|V_{GT}\right| - V_{min}/2\right)\left(1 + \lambda V_{DS}\right)$

where

$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$ (corresponding to *saturation*, *resistive*, and *velocity saturation* modes)

Gate-oxide leakage $I_G = k_1 W \left(V_{ox}/t_{ox}\right)^2 e^{-k_2 t_{ox}/V_{ox}}$

Logic

Shannon's expansion theorem $\overline{f\left(x,\, y,\, z,\, \ldots,\, +,\, \cdot\right)} = f\left(\bar{x},\, \bar{y},\, \bar{z},\, \ldots,\, \cdot,\, +\right)$

Cofactors $f_{\bar{x}} = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=0}$, $f_x = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=1}$

Expansion in sum and product $f\left(x,\, y,\, z,\, \ldots\right) = \bar{x} \cdot f_{\bar{x}} + x \cdot f_x = \left(x + f_{\bar{x}}\right)\left(\bar{x} + f_x\right)$

Observability Don't Care set $\mathrm{ODC}_x = f_{\bar{x}} f_x + \overline{f_{\bar{x}}}\,\overline{f_x}$