Linköping Institute of Technology
Department of Electrical Engineering, Integrated Circuits and Systems

Exam TEN1 in TSTE85 Low Power Electronics

Time:	Thursday 5 April 2018, 14:00–18:00
Place:	TER2
Responsible teacher:	Kent Palmkvist
Allowed aids:	Calculator and appended formula page
Instructions:	Maximum score is 70 p and minimum score to pass is 30 p
Solutions:	Posted on the course web page
Grades:	Posted through LADOK by Monday 23 April 2018
Display:	Time and place will be posted with the grades

1.

a) Describe the impact of average and peak power consumption on a chip design. (2 p)

b) Why is it difficult to estimate the average dynamic power dissipation of a complex circuit like a microprocessor? (2 p)

c) What factors are mainly limiting the power consumption of analog circuits? (2 p)

d) Why is the conventional superheterodyne architecture avoided in power efficient transceivers? (2 p)

e) Consider an adiabatic circuit for which the power clock is high. Explain how a fast transition on the input affects the energy dissipation. (2 p)

f) Low instantaneous power consumption and low average power consumption are important in design of mobile wireless devices. Which two of the following items do mainly affect the average power consumption: *transceiver architecture*, *circuit design*, *power management*, *communication protocols*. (2 p)

2. An outdoor temperature sensor and wireless link consume the power 0.15 mW on average.

a) The energy density of a Lithium-ion battery is 2.4 J/mm^3. How large battery is required to allow for one year of continuous operation if we assume 90% power efficiency? (4 p)

b) A 0.2 mm thick solar cell produces on average 70 W/m^2 when the sun is shining. In the month with least sun, the sun shines 30 hours. Estimate how large solar cell that is needed if it charges the battery with 80% power efficiency. (4 p)

c) How large battery is needed if the solar cell in b) is used? (2 p)

3. An asynchronous design strategy is illustrated in Figure 1.

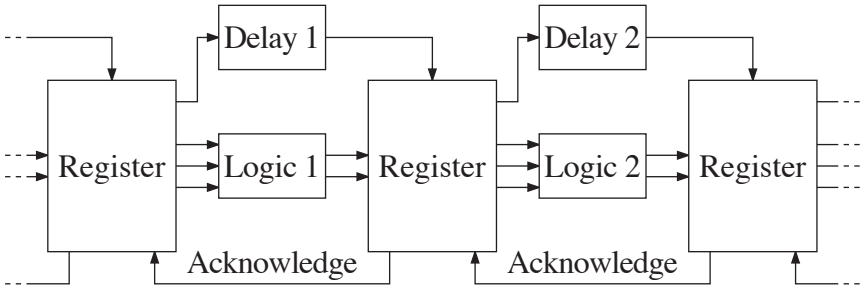

Figure 1. Asynchronous design strategy.

a) Name the strategy. (2 p)

b) How should the timing signal of a delay block be designed? (3 p)

c) State advantages and disadvantages of the asynchronous design strategy over clocked Boolean logic. (4 p)

d) How does null convention logic improve on the asynchronous design strategy above? (3 p)

4. A precharged inverter is shown in Figure 2. The input X has the one's probability P_X, the power supply voltage is V_{DD}, the clock frequency is f_{clk}, and the load capacitance is C_l. A MOSFET has the gate capacitance C_g.

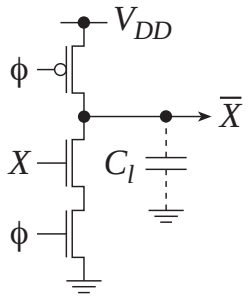

Figure 2. Precharged inverter.

a) Determine the dynamic power consumption required to drive the clock MOSFETs. (2 p)

b) Determine the dynamic power consumption of the circuit. (4 p)

5. The algorithm shown in Figure 3 accumulates an even number of samples N by adding the samples in a sequence $y(n) = x(n) + y(n–1)$; $n = 0, 1, \ldots, N–1$. The register is reset at $n = 0$. The algorithm should be optimized for low energy consumption using algorithm transformations and supply voltage scaling. Assume a constant capacitive load of adders and registers in the implementations, and that the adder and the register hardware operate at a common supply voltage. In a direct implementation of the algorithm in Figure 3 the minimum supply voltage is $V_{DD0} = 1.5$ V.

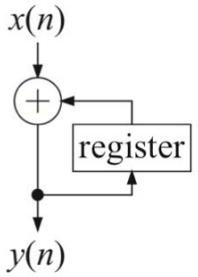

Figure 3. Signal-flow graph of an accumulate algorithm.

a) Transform the algorithm using loop unrolling such that two samples are processed concurrently. Hence the new algorithm should perform the operations $y(2n) = x(2n) + y(2n–1)$ and $y(2n+1) = x(2n+1) + y(2n)$; $n = 0, 1, \ldots, N/2–1$. Draw a signal-flow graph of the new algorithm. (4 p)

b) Use the associative and distributed arithmetic laws to reduce the latency of the critical loop of the algorithm in a). The final latency should equal the sum of one two-input adder and one register delay. Draw the signal-flow graph of the new algorithm. (5 p)

c) Pipeline the algorithm in b) with as few registers as possible so that the throughput becomes limited by the critical loop. (3 p)

d) Assume the same supply voltage V_{DD0} is used in direct implementations of the original algorithm in Figure 3 and the resulting algorithm of c). Estimate the relative energy consumption of the two implementations. (2 p)

e) Minimize the energy consumption of resulting algorithm of c) by scaling the supply voltage. Assume the propagation delay t_p is proportional to $V_{DD}(V_{DD}–V_T)^{-1.5}$ where $V_T = 0.45$ V. Estimate the energy savings after supply voltage scaling relative to a direct implementation of the original algorithm in Figure 3. (4 p)

6. A multiplier with constant coefficient k is interleaved with a factor of 2 according to Figure 4. The lowest power supply voltage for the given clock frequency is V_{DD} = 2.4 V, yielding a total dynamic power consumption P_0.

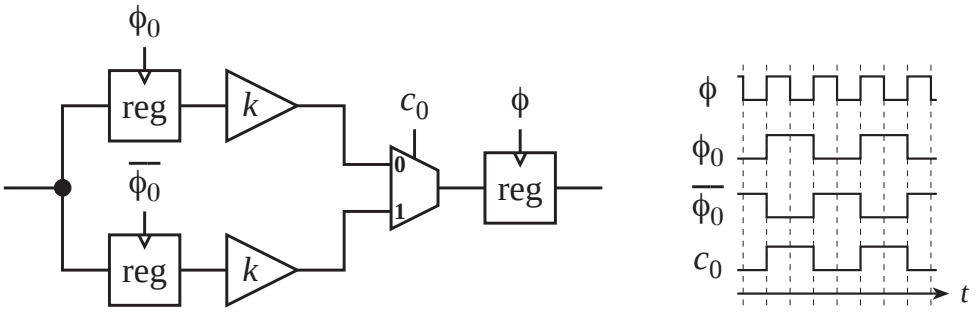

Figure 4. Interleaved multiplier.

a) Redesign the multiplier to use interleaving with a factor of 3. Draw a timing diagram with necessary clock phases and control signals. (4 p)

b) Assume that the new interleaving scheme has not affected the transition activity and that the new multiplexer can be implemented with the same propagation delay. The propagation delay of a register-multiplier-multiplexer branch plotted as a function of the power supply voltage is shown in Figure 5. Use voltage scaling to reduce the new minimal dynamic power consumption. Estimate the power savings. (8 p)

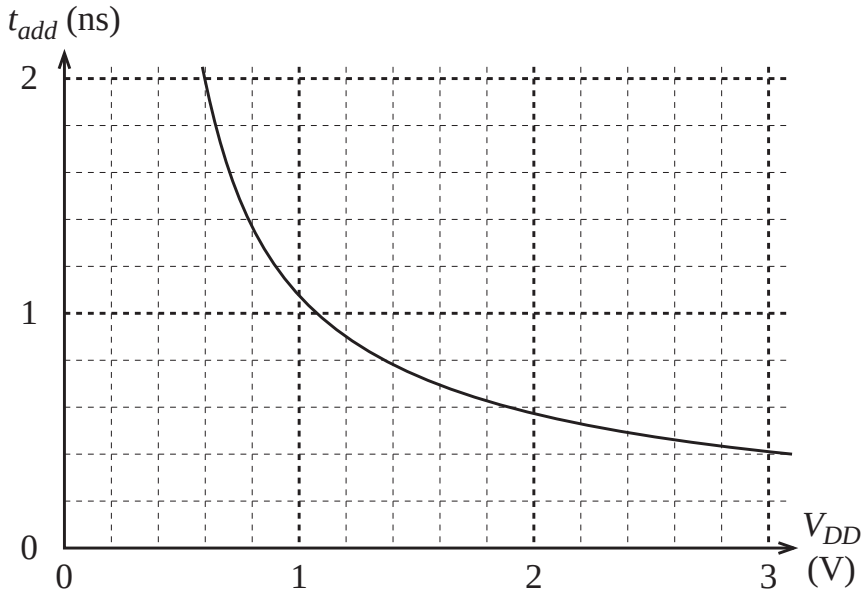

Figure 5. $t_p(V_{DD})$ for a register-multiplier-multiplexer path.

TSTE85 FORMULAS

Circuits

Transition activity $\alpha = \alpha_{01} + \alpha_{10} = 2\alpha_{01} = 2\alpha_{10}$

Switch activity $a = \sum_i \alpha_{01,i} C_i \Big/ \sum_i C_i$

Switched capacitance $C_{sw} = a \sum_i C_i$

Dynamic power consumption $P_d = f_{clk} C_{sw} V_{pp} V_{DD}$

Short-circuit power consumption $P_{sc} = a f_{clk} t_{sc} I_{peak} V_{DD}$

Propagation time $t_p \propto V_{DD} \Big/ \left(V_{DD} - V_T\right)^r$, $1 \le r \le 2$

MOSFETs

Threshold voltage $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$

Weak inversion ($V_{GT} < 0$) $I_D = I_{D0}\left(W/L\right) e^{-\left|V_{GT}\right| / \left(n_s V_\Theta\right)} \left(1 + \lambda V_{DS}\right)$

where

$V_\Theta \approx 26$ mV @ $T = 300$ K

n_s can be calculated from $S = n_s V_\Theta \ln(10)$

Strong inversion ($V_{GT} \ge 0$) $I_D = k'\left(W/L\right) V_{min} \left(\left|V_{GT}\right| - V_{min}/2\right)\left(1 + \lambda V_{DS}\right)$

where

$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$ (corresponding to *saturation*, *resistive*, and *velocity saturation* modes)

Gate-oxide leakage $I_G = k_1 W \left(V_{ox}/t_{ox}\right)^2 e^{-k_2 t_{ox}/V_{ox}}$

Logic

Shannon's expansion theorem $\overline{f\left(x,\, y,\, z,\, \ldots,\, +,\, \cdot\right)} = f\left(\bar{x},\, \bar{y},\, \bar{z},\, \ldots,\, \cdot,\, +\right)$

Cofactors $f_{\bar{x}} = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=0}$, $f_x = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=1}$

Expansion in sum and product $f\left(x,\, y,\, z,\, \ldots\right) = \bar{x} \cdot f_{\bar{x}} + x \cdot f_x = \left(x + f_{\bar{x}}\right)\left(\bar{x} + f_x\right)$

Observability Don't Care set $\mathrm{ODC}_x = f_{\bar{x}} f_x + \overline{f_{\bar{x}}}\,\overline{f_x}$