Lab 2 Power electronics

Contents

Introduction

This lab focus on simulation and evaluation of the full-bridge AC/DC inverter structure. Simulations should be performed, using predefined models.

Tomas Jonsson

LINKÖPING UNIVERSITY
ICS/ISY

Initial setup

The design files used in the lab can be copied from **/site/edu/eks/TSTE19/current/material/Lab2_files** in Linux or from **U:\eks\current\TSTE19\material\Lab2_files** in Windows. Put the copied files into your home directory, for example in /edu/<userid>/TSTE19/ on Linux or H:\TSTE19 on Windows.
Please note that the software only works on Windows. You can thus only run the software in the Freja and Transistorn labs.

Starting the software

The software is started by **Start ->All Programs ->National Instruments ->Circuit Design Suite 14.0 ->Multisim 14.0**
Open the corresponding design project using **File->Open** and select the design file to use among the files you copied in the initial setup.

Notes on the schematics

Some of the schematics have more components added than shown in the tasks in the book. One reason for these (typically small resistances and inductances) are the computational properties of the simulation model. Without the extra components, the simulation calculations could become unsolvable.

Names and values of components can be changed by double-clicking on the value/name. Alternatively, the names and values can be changed by right-clicking on the component and select Properties.

Additional measures can be added by introducing the Measurement probe, which is a yellow symbol at the bottom of the column of symbols on the right side of the window. Place the cursor on top of the symbol to see the name of that particular symbol. Click on it and then click on a wire in the schematic to add a measurement probe to the schematic.

One useful variable for the following analysis step is a time variable. The Multisim environment does not directly support such a variable, but it can easily be added in one of many ways. The approach taken in the existing simulation models are the use of voltage source that increments its output voltage linearly at the rate of 1 V per second. The voltage value is then the same as the time value, as long as the maximum time is not exceeded.

Simulating the design

Simulation of the design can be done using different analysis configurations. The ones used in this lab will be transient and Fourier analysis.

The analysis (and simulation) of the design is started by selecting **Simulate->Analysis->Transient analysis** or **Simulate->Analysis->Fourier analysis** respectively. This will start the simulator, which will store the waveforms of all nodes in the circuit for future presentation. The simulator opens a new window named Graph View, in which all waveforms are presented.

Existing simulation variables

All voltages and currents in the circuit are available after simulation. The voltages at individual nodes are accessed using the names V(1) etc. All nodes are either named explicitly or enumerated and shown as a red text or digit in the schematic. I(Rs) gives the current entering Rs. The currents usually are assuming the positive current entering the 1st pin of the symbol.
Plotting the voltage across a given component is then done by calculating the voltage difference between the node voltages the component is connected to.

Extra measurement points

Additional measurements of voltage and current can be added through placing probes in the Multisim circuit by selecting

Place->Probe->Voltage (Current or Differential voltage).

OBS these probes cannot be used for harmonic Fourier analysis.

Presentation and analysis of the result

The Graph View window presents the waveforms of some selected voltages and currents. Individual traces can be disabled by deselecting the corresponding white box at the bottom of the window.

New traces can be added using **Graph->Add trace(s)** from latest simulation result. In the resulting dialog window additional traces can be added to the existing graph, or to a new graph. Select the trace of interest, press Copy variable to expression, then press Calculate.

Beside currents, node voltages and power traces, additional traces can be calculated using mathematical expression. Among the simplest examples of this is the calculation of the voltage across a component. E. g., if a component is connected between nodes 3 and 5 (assuming + on node 3), the voltage across that component is then calculated using the expression V(3) – V(5).

Other functions may also be used, such as **RMS** and **AVG**, which calculates the rms and average values respectively of a signal or expression. Example: **RMS(V(1))**.

Note that these calculations is made on the calculated waveform, and is therefore different at different times, as the calculation is not performed on an infinite long waveform.

Arbitrary mathematical functions can also be plotted by the use of a time variable (using

the voltage of a triangle wave voltage source). A sinusiodal waveform of 10 V, 50 Hz with a phase shift of 45 degrees can be plotted using the trace entry 10*sin(2*pi*50*V(time)+45*pi/180). Note that the angles are always described in radians.

The Fourier transform can be calculated on signals and expressions. Select Simulate->Analysis->Fourier analysis. Set the fundamental frequency, number of harmonics, and stop time for sampling. Select the output tab, and add there the variables and expressions that will have their Fourier series coefficients calculated. Finally, press Simulate. The simulation is now run, and the simulation result is used to calculate the Fourier series coefficients and then present them together with details about DC component and distortion factor THD in the Graph View window.

Waveform results can be copied using **Edit->Copy** graph to clipboard and then pasted into a LibreOffice or Wordpad document or Paint for editing.

Lab 2-1 Ideal full-bridge inverter with unipolar switching

Multisim model

Load the model FB_inv_unipol.ms4.

Circuit description

A single phase inverter as shown by Figure 1, will be rated and analyzed in this lab task. The converter is feeding an ac-source through an inductance, which could correspond to an induction motor alternatively a grid connected converter connecting a PV-panel.

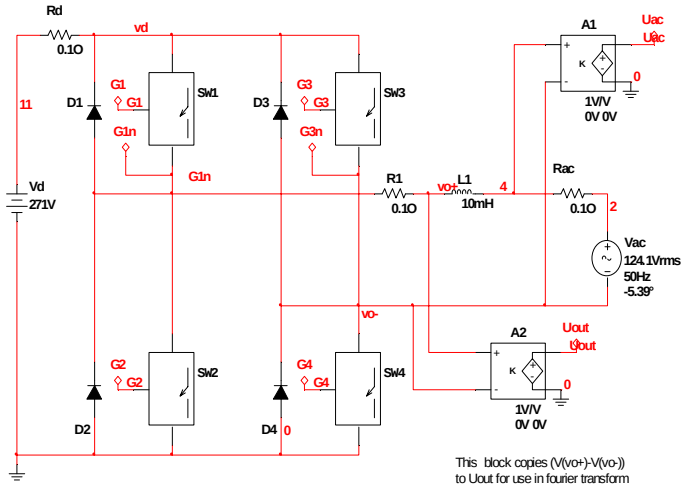

Figure 1 Full-bridge converter with ideal switches

The converter model used in this task contains ideal switches and diodes in order to obtain fast simulation. The switch-model is presented in Figure 2 below, which shows an ideal switch in series with a diode. The model resembles e.g. a MOSFET where IO1, IO2 and IO3 corresponds to drain, gate and source, respectively. The voltage between gate and source (IO2-IO3) shall be 1 V to turn-on the switch.

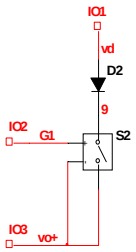

Figure 2 Switch model

The pulse width modulation used here is unipolar with a switching frequency of 950 Hz. This gives a frequency modulation ratio of 19, related to the fundamental frequency of 50 Hz. The PWM is defined as shown by Figure 3, giving the gate signals G1-G4 to define the turn-on and turn-off of the switches.

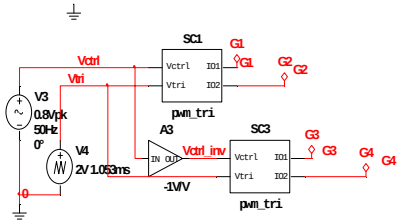

Figure 3 Unipolar PWM control

The PWM reference is defined by the signal Vctrl, which has an amplitude corresponding to the desired amplitude modulation index, m_a. In Figure 4 below the signal Vctrl and the PWM carrier, Vtri is shown.

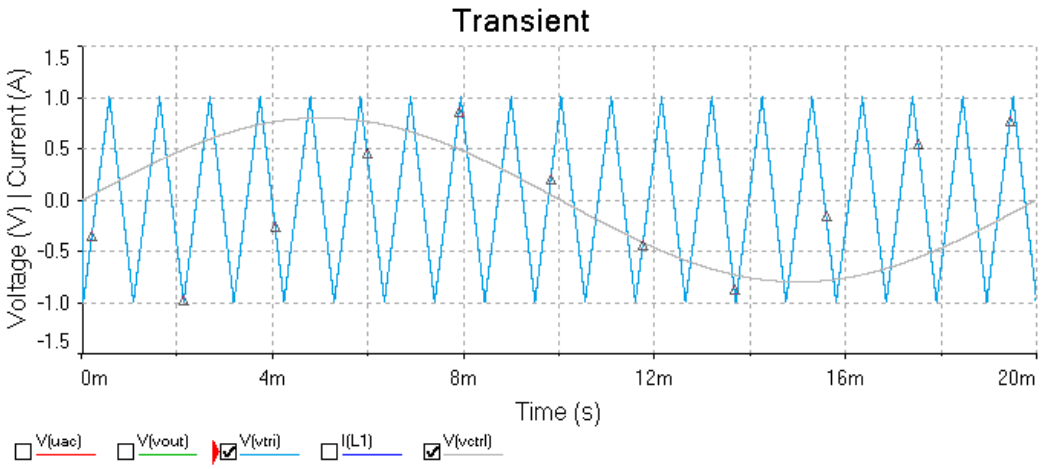

Figure 4

Looking inside the blocks SC1 and SC3 reveals the creation of the Gate pulses. Here the output signals IO1 and IO2 correspond to G1 and G2 in block SC1 and G3 and G4 in block SC3, respectively.

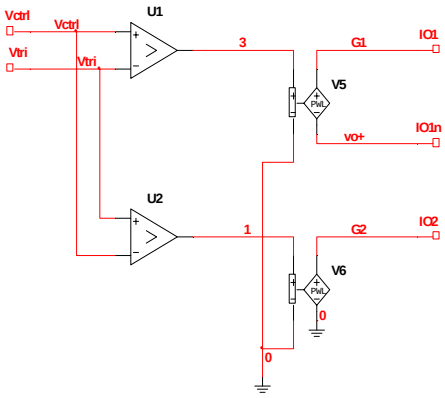

Figure 5 Gate pulse generation

The time instant of the gate pulse is defined by the comparators U1 and U2 which changes from logical 0 to a logical 1 output when the signal Vctrl exceeds Vtri. The gate signals G1 and G2 shall generally be the inverse to the other. However, in order to ensure both switches in a leg is conducting simultaneously, a blanking interval is introduced. The blanking implies, that the turn-off of one switch is done before turning on the other as shown below.

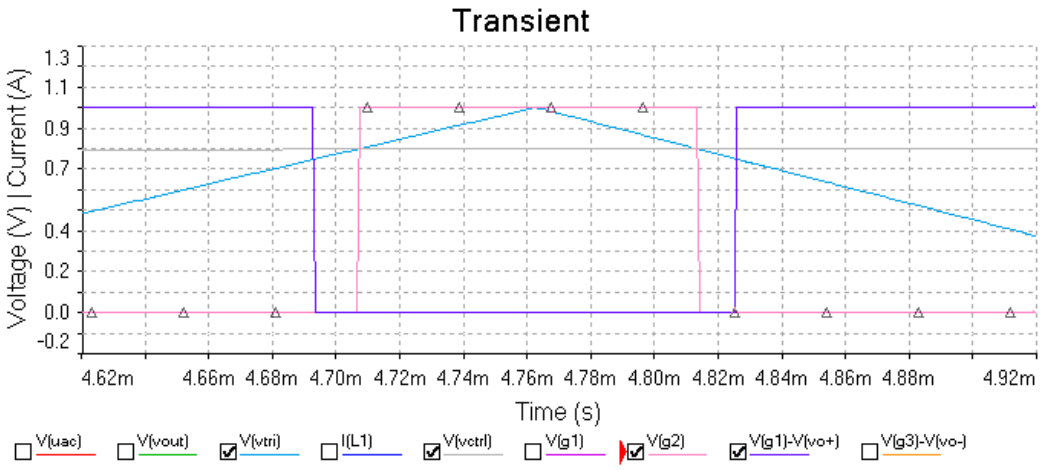

Figure 6

The blanking is accomplished in this case by introducing an offset in comparator U1. The final gate pulses that are connected to the switches of the converter from the PWM circuit is sent through voltage controlled voltage generators in order to overcome the potential shift of switch 1 and 3 (Sw1 & SW3). The lower terminal of Sw1 (G1n) will when Sw2 is off, be at a potential corresponding to Vd. In Figure 6 above the voltage signal between G1 and G1n is shown together with G2. G2 connection to Sw2 (and G4 to Sw4) does not pose any problem with potential shift since these lower switches are connected with the source directly to ground.

Lab 2-1 Converter design

The model in FB_inv_unipol.ms4 shall be updated with respect to the circuit parameters. Follow the design steps listed below:

1. Ac-voltage: Vac1 = 230 Vrms, 50 Hz, 0 deg
2. Select a dc-voltage, Vd, to get ma=0.9 at the given ac-voltage.
3. Define the rated fundamental ac-side current, Iac1, corresponding to 2000 VA (2000 W at cos(fi)=1)
4. Define a series inductance giving 10% of the base impedance ($Z_b = \frac{V_{ac1}}{I_{ac1}}$) at 50Hz. $X_L = 0.1\ Z_b$
5. Set the PWM reference (Vctrl) for m_a=0.9 and a phase angle = 0.

Lab 2-1 Design calculations

Calculate the magnitude and phase of the fundamental current component on the ac-side. Consider the following equation:

$$\frac{\hat{U}_{out}e^{j\varphi_{out}} - \hat{U}_{ac}e^{j\varphi_{ac}}}{j\omega L}$$

Lab 2-1 Measurements

Using the model with the modified converter parameters above, perform the following measurements:

1. Magnitude and phase of the fundamental frequency ac-side current component (current through L1).
2. Peak ac-side current I(L1).
3. Magnitude and phase of the fundamental frequency component of the switched output voltage, Vout.
4. Spectra of Vout. Use Fourier function to get up to the 100th harmonic.
5. Spectra of ac-current through L1. Use Fourier function to get up to the 100th harmonic.
6. Calculate active and reactive power that is fed into the ac-source (Vac).
7. Change PWM reference (Vctrl) to get P=2kW and Q=0Var into the ac-source.

Reference

Section 8-3-2 in Mohan Power electronics

Lab 2-2 MOSFET based full-bridge inverter with optimized gate drive

This task relates to a single phase full-bridge inverter similar to the one analysed in task 2-1 above. This inverter is however based on detailed MOSFET and diode models and with a more sophisticated gate drive circuitry.

A Multisim model is found in the Lab2 system folder as: inv_lab2.ms14

The Multisim model also needs the two additional files: Inverter_circuit_Lab2.ms14 and NonOverlapping_Lab2.ms14 for definition of sub-circuits. Note that only the main file needs to be loaded, the two additional files shall reside in the same folder.

The model is hierarchical with the top level shown below. The top level includes control references, the PWM control and the physical inverter circuit.

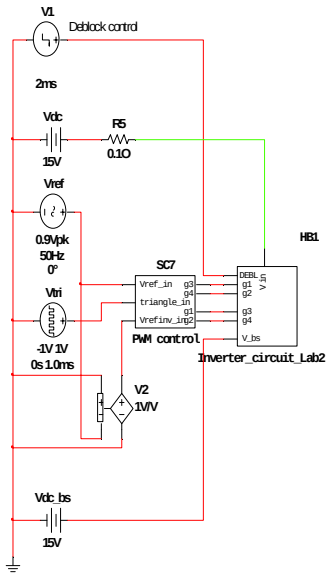

Figure 7 Front end with control references for the full-bridge inverter

PWM control

The PWM control is given by the PWM control block as shown by Figure 8 below.

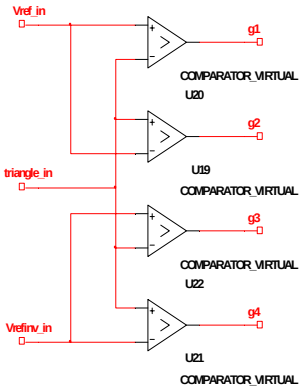

Figure 8 PWM control

The PWM is setup for unipolar switching where G1 and G2 corresponds to one leg of the full-bridge converter and G3 and G4 of the other. The gate pulse G1 and G2 are derived using the Vref_in signal while G3 and G4 referred to the inverse Vrefinv_in. Blanking time is included through an offset of -0.05 in the comparators of G1 and G3. Thereby the following expressions can be written corresponding to the gate pulse generation:

G1 = Vref_in-0.05 > triangle_in

G2 = triangle_in > Vref_in

G3 = Vrefinv_in-0.05 > triangle_in
G4 = triangle_in > Vrefinv_in

Through the addition of the negative offset to Vref for G1 a blanking interval is obtained with respect to G2. This is explained by the fact that for increasing triangle wave, the intersection with Vref will come earlier through the negative offset, resulting in G1 turn-off earlier than the G2 turn-on. The opposite applies to interval with decreasing triangle wave, where the negative offset will delay the intersection with Vref, resulting in a later G1 turn-on compared to the G2 turn-off.

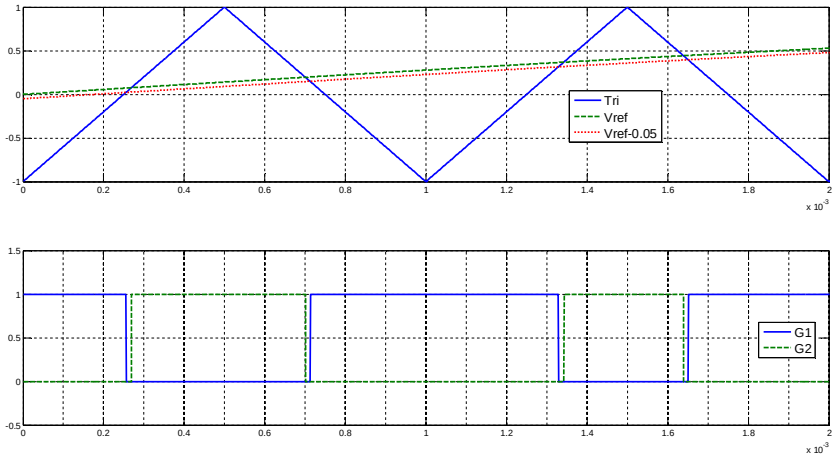

Figure 9 PWM

The blanking time obtained with the offset is defined by the rate of change of the triangle wave according to the following equation:

$$t_{blank} = \frac{|offset|}{dV_{tri}/dt} = \frac{|offset|}{4f_s}$$

For f_s = 1 kHz and an offset = -0.05 a blanking time of 12.5 µs is obtained.

Firing pulse interlocking

The next block after PWM control is “NonOverlapping” and contains logic to obtain interlocking between G1/G2 and G3/G4 to prevent simultaneous on-state. When G1 is on, G2 must equal zero in order to permit turn-on through G1. The same applies to the other combinations of G1 – G4. The logic also contains a deblock signal which when equal to zero sets all gate pulses to off-state. Enabling of normal switching is done with deblock=1.

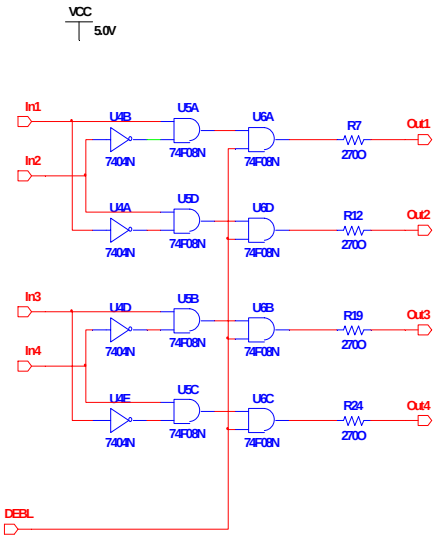

Figure 10

Gate drive circuits

The PWM gate pulses are converted into the final gate-source voltage through the circuit showed below:

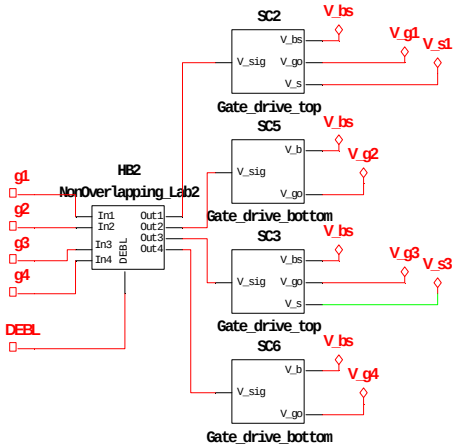

Figure 11

The gate drive blocks provide isolation in addition to the actual driving of the required gate current for the proper turn-on and turn-off.

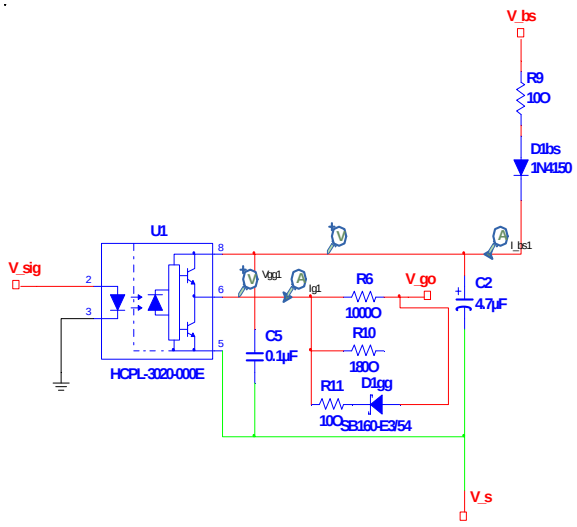

Figure 12 Gate drive of upper switches (Q1 & Q3)

Isolation is provided through the opto-coupler U1 of the type HCPL-3020 by AVAGO Technologies. The data sheet is found in the Lab2 system folder.
The supply to the gate drive is provided by the bootstrap circuit constituted by R9, D1bs and C2 in Figure 12. Bootstrapping is required since the upper switches will see a potential of the source (and gate) that changes through the switching operation. The bootstrap is fed by the dc-voltage source Vdc_bs in Figure 7. Charging of the bootstrap capacitor C2 will commence at the initial turn-on of the main switch Q2 (see Figure 15). The initial charging current will be limited by R2, which also sets a time constant together with the capacitor which defines the speed of charging.

The gate drive provides separate gate resistance for turn-on and turn-off. Turn-on is determined by R6 (can be paralleled by R10) and turn-off by R11 in series with the schottky diode D1gg.

The gate drive for the lower switches Q2 and Q4 does not need the bootstrap circuit due to grounding of the source terminals, allowing the drive circuit to be connected to a normal voltage supply.

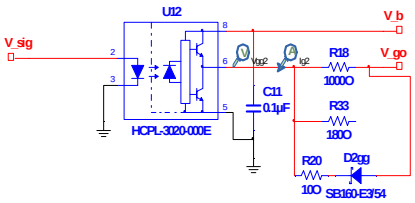

Figure 13 Gate drive for lower switches (Q2 & Q4)

Inverter main circuit

The full-bridge inverter circuit is defined by the "Inverter_core" block in Figure 14, where the following external terminals are found:

V_in: The dc-side voltage
V_op: The positive ac-output terminal
V_on: The negative ac-output terminal

The load is connected between V_op and V_on.

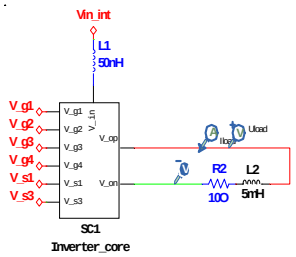

Figure 14

Inside "Inverter-core" the detailed full-bridge inverter circuit is defined as shown by Figure 15

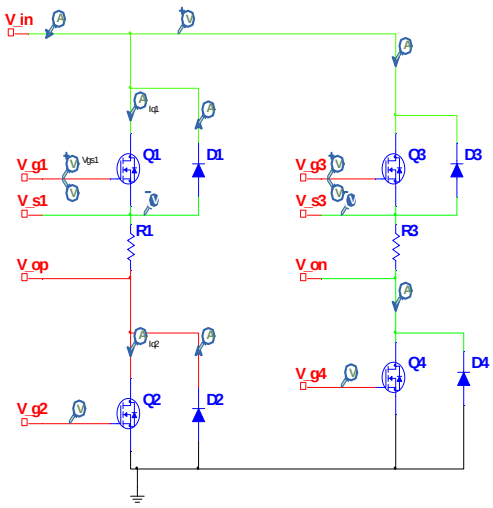

Figure 15 Full-bridge inverter circuit

The full-bridge is designed with MOSFET switches Q1-Q4 of type IRF540 by VISHAY. An antiparallel diode is included with each MOSFET as D1-D4 of the type BYW29E-200. The data sheets for the MOSFET and the diode is found in the Lab2 system folder.

Lab 2-2 Performance calculations

Related to the design presented for the MOSFET based full-bridge inverter, perform the following calculations of some performance parameters:

1. Total initial inrush current into the bootstrap supply. Neglect the current to the opto-isolated drive circuits HCPL-3020.
2. Time delay from deblock until normal switching. Check HCPL-3020 datasheet for minimum supply voltage level for startup. Check the first switching instant of Q2 and Q4.
3. Total turn-on delay related to drive circuit parameters (Rg, HCPL-3020 output voltage and delay) and MOSFET gate charge. Use datasheets for reference. Consider the following definitions of device capacitances.
    a. $C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted
    b. $C_{rss} = C_{GD}$
    c. $C_{oss} = C_{DS} + C_{GD}$
4. Calculate the dv_{ds}/dt (drain-source voltage) during turn-on. Consider MOSFET capacitance data for Vds=10V.
5. Calculate the total parasitic raise of Vgs for a MOSFET in off-state when the opposite switch is turning on. Assume the V_{ds} of the MOSFET to be exposed by a positive dv_{ds}/dt as calculated in step 4 above. Consider the entire gate circuit from the HCPL-3020 driver to the MOSFET. The actual output voltage of the HCPL-3020 corresponding to off-state is given in the datasheet.

Datasheets

The following data sheets and application notes are available at the Lab2 system folder:

[1] AN-6076, Design and application guide of bootstrap circuit for high-voltage gate drive IC
[2] BYW29E-200, Ultrafast power diode
[3] HCPL-30200302-04-Amp-Output-Current-IGBT-Gate-Drive-Optocoupler
[4] IR MOSFET basics
[5] IRF540, Power MOSFET
[6] Power MOSFET basics VISHAY

[7] SB160 Schottky barrier rectifier

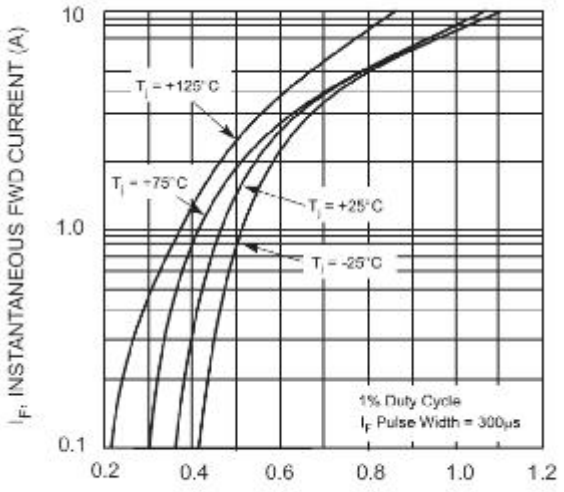

Fig. 2 Typical Forward Characteristics - SB120 thru SB140

Figure 16