7 Operational Amplifiers II

Part 7.A—Repetition

Single-pole and dual-pole systems

General approximation of a multi-pole system:

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right) \cdot \left(1 + \frac{s}{p_q}\right)}$$

Zeros and poles are approximated by an equivalent pole p_q. If we have a second pole dominating over other higher poles, $p_q \approx p_2$ $(p_q > p_2)$.

A two-pole system in a feedback loop

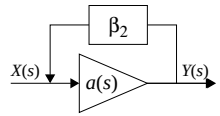


Figure 7.1: Amplifier with feedback.

"Optimal" behavior (bandwidth usage) for $Q = 1/\sqrt{2}$ gives a phase margin $\varphi_m \approx 67°$. Design goal should be in the order of 75 degrees in order to have a proper design margin.

Design requirements put on the phase margin, the equivalent pole, and the Q-value.

The Q-value is also given by the feedback factor β:

$$Q \sim \sqrt{\frac{\beta \cdot A_0 \cdot p_1}{p_q}}$$

Passive compensation

Introduce a capacitance C_c between the output of the stages. We have that the first pole now ends up at

$$p_1 \approx \frac{g_I \cdot g_{II}}{g_{mII} \cdot C_c}$$

Hence the pole is moved down and this is referred to as the Miller effect. Sometimes we refer to this kind of capacitance as the Miller capacitance.

We also have that the second pole is linearly dependent on the g_{mII}, and

$$p_1 \sim \frac{1}{g_{mII}} \text{ and } p_2 \sim g_{mII}$$

This is referred to as pole splitting.

The Miller compensation introduces a zero in the RHP which destroys the phase. This can be removed by adding a resistance in series with the capacitance:

$$R_c + \frac{1}{sC_c}$$

The zero can now be cancelled by either letting it move towards infinity or to cancel the second pole p_2. This calls for two different options:

$$R_c = \frac{1}{g_{mII}} \text{ or } R_c = \frac{1}{g_{mII} \cdot C_c} \cdot (C_I + C_{II} + C_c)$$

The latter is referred to as pole-zero cancelling.

Part 7.B—High-performance operational amplifiers

The difference between the OTA and the OP is given by the fact that the operational amplifer should have a zero output impedance whereas the OTA should have an infinite output impedance.

The difference between the Gm and the OTA is given by the fact that the Gm should have a fixed transconductance value over a large input voltage range. Therefore linearization circuits are mostly needed.

Basically if we are driving capacitive loads only, OTAs and OPs can be used. Therefore, we can increased the output impedance in order to increase the gain for high accuracy applications.

If a low output impedance is needed, the output current may be increased in order to reduce the output impedance or a there is a need for an additional source-follower at the output to lower the output impedance.

Basically: How can we achieve high p_1, high A_0 at the same time as p_2 (p_q) is much more higher (improved phase margin)?

Part 7.C—Two-stage amplifier

Consider the compensated two-stage amplifier in the figure.

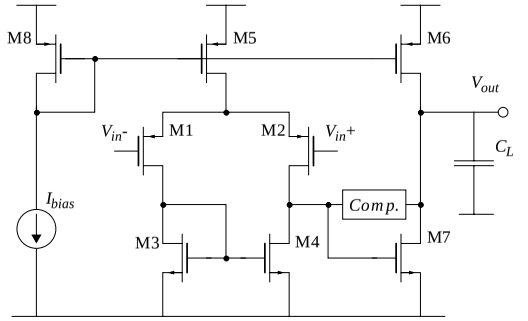


Figure 7.2: A two-stage OP/OTA with compensation circuit.

The output from the first stage is connected to a high-impedance node at the input of the first stage (high R and high C). Therefore, the poles are poorly separated.

$$p_1 = \frac{g_{ds}^2}{g_{mII} \cdot C_c} \text{ and } p_2 = \frac{g_{mII} C_c}{C_c C_I + C_c C_{II} + C_I C_{II}} \approx \frac{g_{mII}}{C_I + C_{II}}$$

$$z = \frac{1}{g_{mII}/C_c}$$

$$\omega_u = \frac{g_{mI}}{C_c}$$

$$\text{SR} = \min\left\{\frac{I_5}{C_c + C_I}, \frac{I_6}{C_c + C_{II}}\right\}$$

(We only consider Miller compensation). We find that we can increase the p_2 by increasing g_{mII}. If we increase the area of the transistor (W) the capacitance C_I will however increase even faster and then the p_2 will in fact *decrease*.

Design issues

- Systematic offset
- Distribute the gain in the two stages so that the Miller effect and p_2 are controlled.
- Insensitive to load capacitance due to the compensation capacitance and the pole splitting.
- Controlled DC voltages (equal input and output voltages possible)
- Low-voltage operation.
- Poorly separated poles (compensation often required).

Part 7.D—Telescopic-cascode amplifier

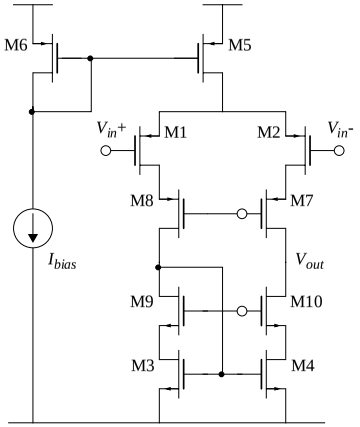


Figure 7.3: A telescopic-cascode OTA.

One-stage amplifier with low impedance nodes. High output impedance in order to increase DC gain and the poles become well-separated poles

$$p_1 = \frac{2 \cdot g_{ds}^2}{g_{m7} C_L} \text{ and } p_2 = \frac{g_{m7}}{C_{gs7} + C_{gd1} + C_{b7}}$$

$$\omega_u = \frac{g_{m1}}{C_L}$$

$$\text{SR} = \frac{I_5}{C_L}$$

Design issues

- Gain in one stage only – simpler design
- Sensitive to load capacitance
- Equal input and output DC voltages not feasible
- High-voltage operation
- Well separated poles

Part 7.E—Folded-cascode amplifier

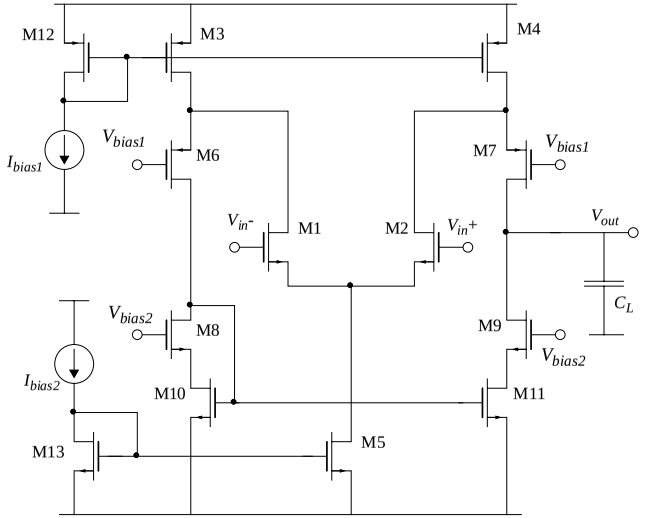


Figure 7.4: A folded-cascode amplifier.

One-stage amplifier with internal low impedance nodes. High output impedance in order to increase DC gain and the poles become well-separated poles

$$p_1 = \frac{g_{ds}^2}{g_m C_L} \text{ and } p_2 = \frac{g_{m7}}{C_{gs7} + C_{gd4} + C_{gd4} + C_{b7}}$$

$$\omega_u = \frac{g_m}{C_L}$$

$$\text{SR} = \frac{I_4}{C_L}$$

Design issues

- Sensitive to load capacitance
- Controlled DC voltages (equal input and output voltages possible)
- Low-voltage operation possible
- Well separated poles due to high output impedance
- Choose $I_1 \approx 4 \cdot I_7$. We have $I_5 = 2 \cdot I_1$ and $I_4 = I_1 + I_7$, which gives that $I_4 = 5 \cdot I_7 = \frac{5}{8} I_5$.

Part 7.F—Current-mirror amplifier

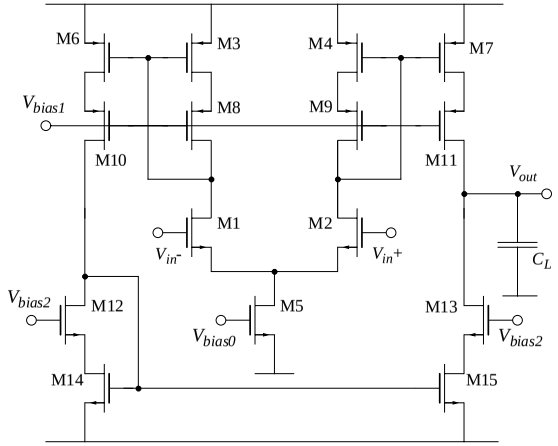


Figure 7.5: A current-mirror amplifier.

One-stage amplifier with internal low impedance nodes. High output impedance in order to increase DC gain and the poles become well-separated poles

$$p_1 = \frac{g_{ds}^2}{g_m C_L} \text{ and } p_2 = \frac{g_{m4}}{C_{gs4} + C_{gs7} + C_{gd6} + C_{gd8} + C_{gs9} + C_{b4}}$$

$$\omega_u = \frac{K \cdot g_{m1}}{C_L}$$

$$\text{SR} = \frac{K \cdot I_5}{C_L}$$

Design issues

- Sensitive to load capacitance
- Controlled DC voltages (equal input and output voltages possible)
- Low-voltage operation possible
- Well separated poles due to high output impedance
- $I_1 \approx 4 \cdot I_7$ gives that $I_4 = I_1 + I_7 = 5 \cdot I_7$. $I_5 = 2 \cdot I_1$. $I_4 = 2.5 \cdot I_5$.

Part 7.G—Fully-differential amplifers

Assume that we have a non-linear transfer function

$$V_{out} = a \cdot V_{in} + b \cdot V_{in}^2 + c \cdot V_{in}^3 + d \cdot V_{in}^4 + \ldots$$

Again assume that we have a positive and negative input through this system (consider the AC signals):

$$V_{out}^+ = a \cdot V_{in}^+ + b \cdot (V_{in}^+)^2 + c \cdot (V_{in}^+)^3 + d \cdot (V_{in}^+)^4 + \ldots \text{ and}$$
$$V_{out}^- = a \cdot V_{in}^- + b \cdot (V_{in}^-)^2 + c \cdot (V_{in}^-)^3 + d \cdot (V_{in}^-)^4 + \ldots$$

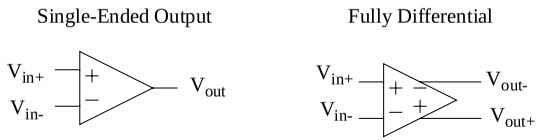
The difference between the output signals is

$$V_{out,\,diff} = V_{out}^+ - V_{out}^- = a \cdot (V_{in}^+ - V_{in}^-) + b \cdot ((V_{in}^+)^2 - (V_{in}^-)^2) + \ldots$$

If we assume that the input signals are perfect, hence $V_{in}^+ = -V_{in}^- = V_{in}$, we have that

$$V_{out,\,diff} = 2a \cdot V_{in} + 2c \cdot V_{in}^3 + \ldots$$

Hence only the odd terms are left and even terms are eliminated. Therefore, using differential signals, we have a gain in performance (linearity).



gure 7.6: Differential operational amplifier.

The differential input and output voltages are given by

$$\Delta V_{in} = V_{in}^+ - V_{in}^- \text{ and } \Delta V_{out} = V_{out}^+ - V_{out}^-$$

The common-mode input and ouptut voltages are given by

$$\nabla V_{in} = \frac{V_{in}^+ + V_{in}^-}{2} \text{ and } \nabla V_{out} = \frac{V_{out}^+ + V_{out}^-}{2}$$

The output voltages (or the transfer function) are given by

$$\begin{bmatrix} \Delta V_{out} \\ \nabla V_{out} \end{bmatrix} = \begin{bmatrix} A_d & A_{cm} \\ x & x \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{out} \\ \nabla V_{out} \end{bmatrix}$$

We consider the differential gain and the common-mode gain.

Common-mode feedback circuit, CMFB

Poor gain of the common-mode signal in the feedback loop and therefore we need a special feedback circuit in order to achieve high common-mode gain and hence stabilize the common-mode voltages.

The input voltages of the CMFB are the positive and negative output voltages from the differential amplifier. We have that the output voltage (or current) *should be a function of the common-mode signal and not a function of the differential signal*.

Examples (see Johns&Martin for illustrative examples):

gure 7.7: Continuous-time CMFB circuits.