Lecture 9, ANIK

Data converters 1

LiU EXPANDING REALITY

What did we do last time?

Noise and distortion

- Understanding the simplest circuit noise
- Understanding some of the sources of distortion

What will we do today?

Data converter fundamentals

- DACs
- ADCs
- Transfer characteristics
- Error measures
- Typical architectures

Data converters fundamentals

DAC

- Represents a digital signal with an analog signal
- To control something
- To transmit something (a modulated signal)

ADC

- Represents an analog signal with a digital signal
- To measure something
- To receive something (a modulated signal)

And there are others:

- Time-to-digital converters
- Frequency-to-digital converters
- etc.

The quantization process

Distinct levels can be detected (ADC)/represented (DAC)

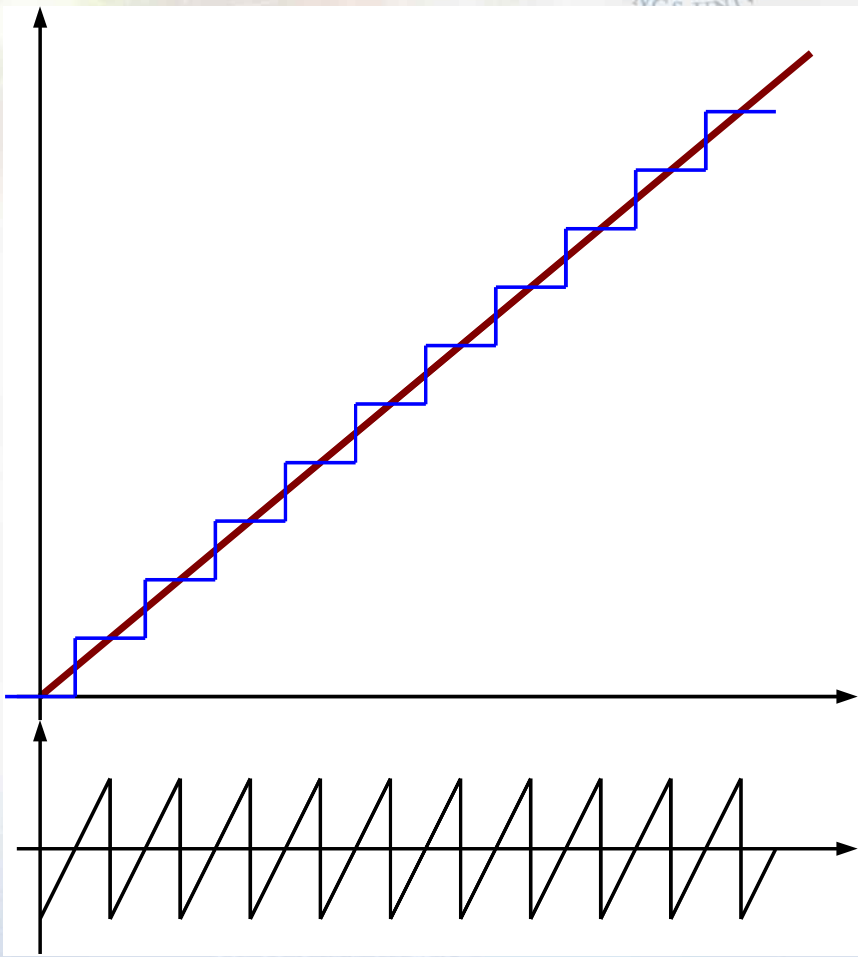
The quantization error is the deviation from the straight line

Range is 0 to V_{ref}, which gives stepsize

$$\Delta = \frac{V_{ref}}{2^N}$$

The quantization error is bounded (as long as we do not saturate):

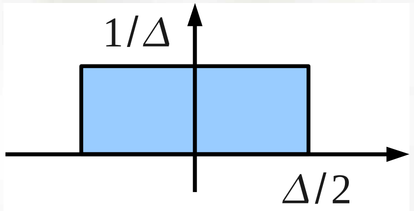
$$Q \in \left[-\frac{\Delta}{2}, \frac{\Delta}{2} \right]$$



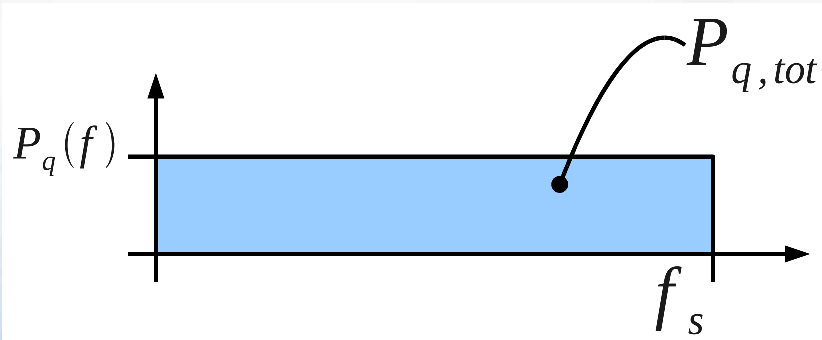
Quantization process, cont'd

Assume signal-independent (not true for a low number of bits)

- Quantization assumed to be a stochastic process
- Assume white noise, uniformly distributed in $\{-\Delta/2, \Delta/2\}$



Noise power spectral density



Quantization process, cont'd

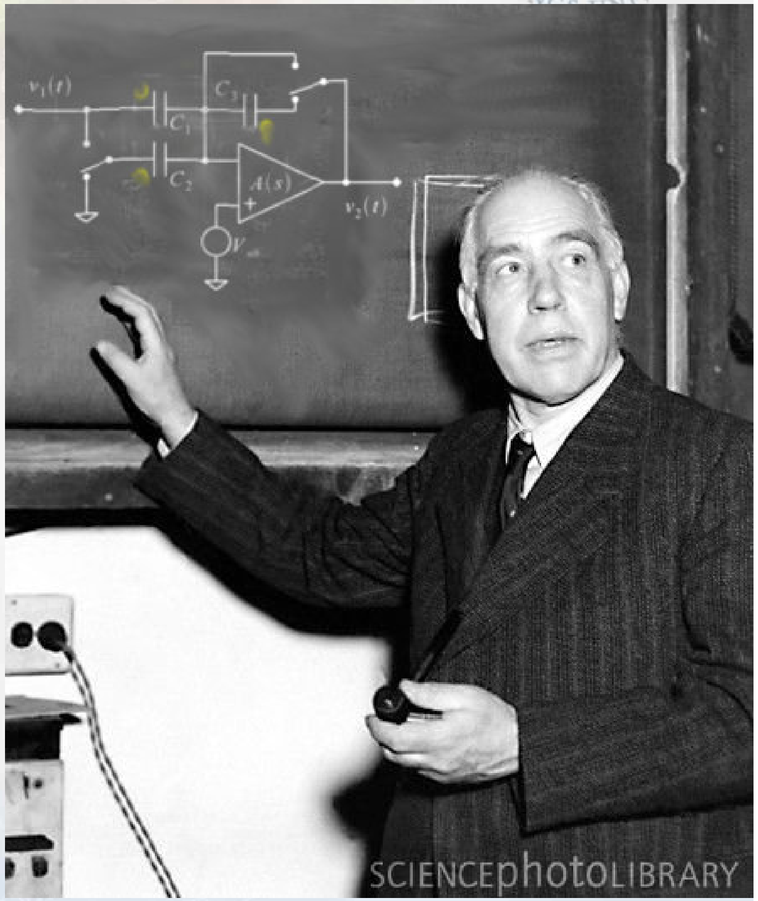
Sigma of the probabilistic noise

Noise model

- Remember the superfunction

Power spectral density

- A certain bandwidth contains a certain amount of noise



Quantization process, cont'd

Peak power assuming centered around the nominal DC level

$$P_{pk} = \left(\frac{V_{ref}}{2} \right)^2$$

Maximum, average sinusoidal power

$$P_{avg} = \frac{1}{2} \cdot \left(\frac{V_{ref}}{2} \right)^2 = \frac{1}{8} \cdot V_{ref}^2 = \frac{P_{pk}}{2}$$

Peak-to-average ratio (PAR) for a sinusoid

$$\mathrm{PAR} = \frac{P_{pk}}{P_{avg}} = 2$$ (1.76 dB)

Quantization process, cont'd

Noise power given by the sigma: $P_{q,tot} = \sigma^2 = \frac{\Delta^2}{12}$

Signal-to-quantization-noise ratio: $\mathrm{SQNR} = \frac{P_{avg}}{P_{q,tot}} = \frac{P_{pk}}{P_{q,tot} \cdot \mathrm{PAR}}$

With values inserted

$$\mathrm{SQNR} = \frac{\frac{1}{4} \cdot V_{ref}^2}{\frac{1}{12} \cdot \left(\frac{V_{ref}}{2^N} \right)^2 \cdot \mathrm{PAR}} = \frac{3 \cdot 2^{2N}}{\mathrm{PAR}}$$

In logarithmic scale

$\mathrm{SQNR} \approx 6.02 \cdot N + 4.77 - \mathrm{PAR} = 6.02 \cdot N + 1.76$ for our sinusoid.

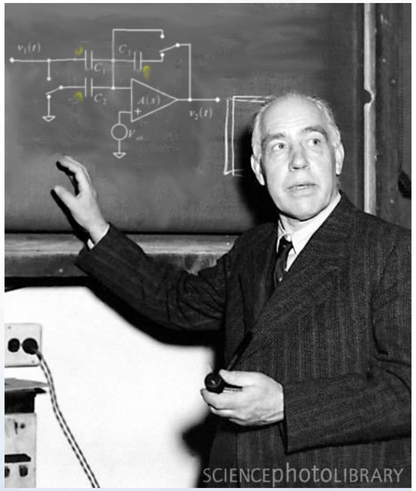
D/A conversion as such

Amplitude is generated by scaling the digital bits and summing them

$$A_{out}(nT) = \sum_{k=0}^{N-1} w_k(nT) \cdot 2^k$$

The scaling does not necessarily have to be binary:

- Binary
- Thermometer
- Linear
- Segmented



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D/A conversion, cont'd

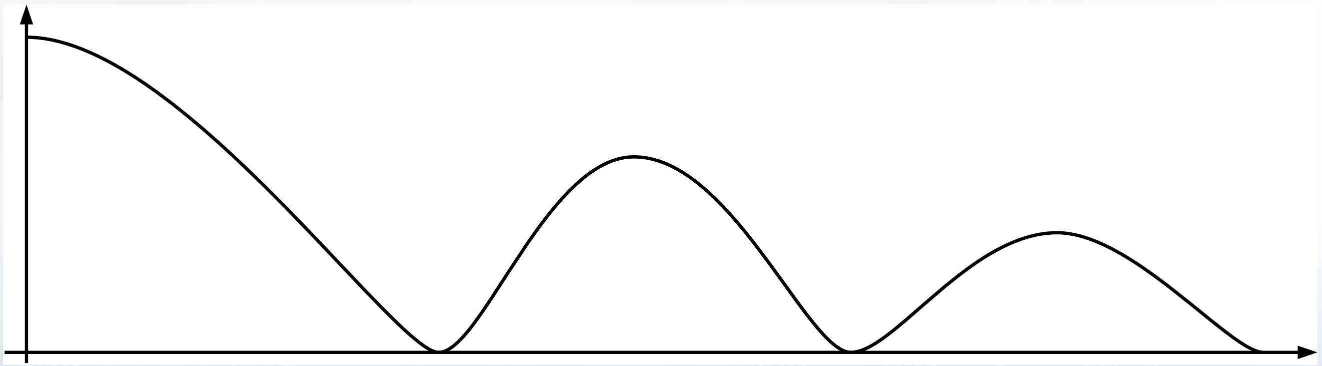
The output is a pulse-amplitude modulated signal (PAM)

$$A_{out}(t)=\sum a(nT)\cdot p(t-nT)$$

such that the spectrum is

$$A_{OUT}(j\omega)=A\left(e^{j\omega T}\right)\cdot P(j\omega)$$

A common pulse is the zero-order hold, since ideal reconstruction is impossible. In the frequency domain the output will be sinc-weighted:



A reconstruction filter is needed to compensate!

D/A converter architectures

Current-steering

Outputs summed by weighted current sources. KCL simplifies this

Switched-capacitor (MDAC)

An SC gain circuit with weighted capacitors, c.f. the multiple input OP gain circuit

Resistor-string

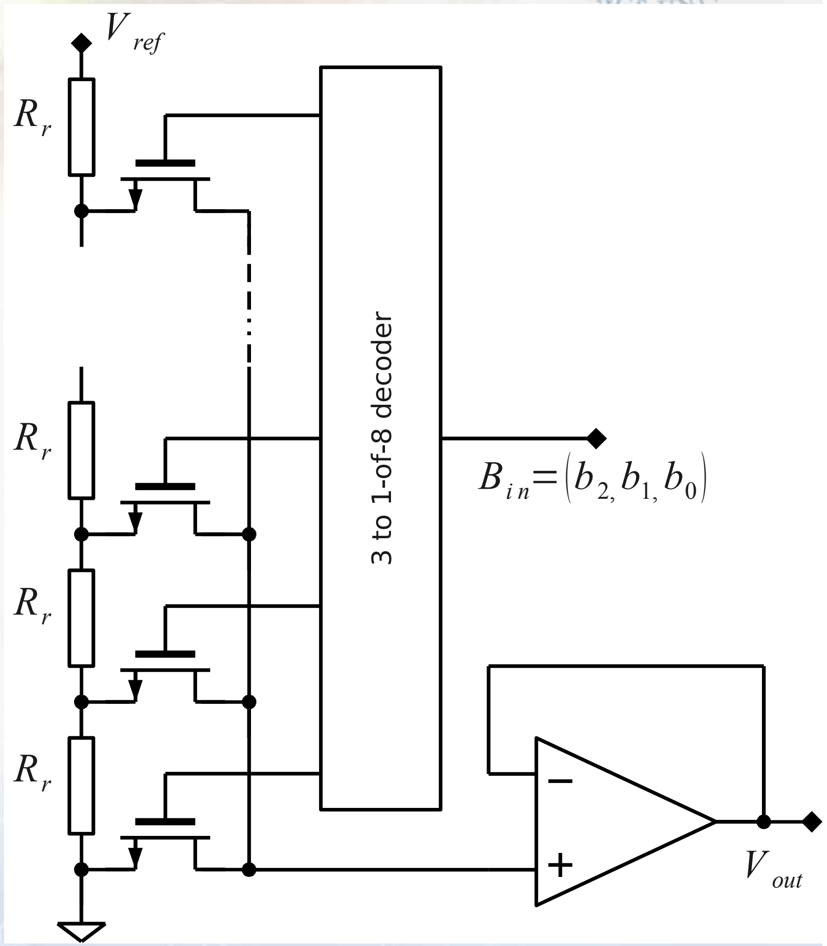
Select a certain tap out of many and buffer to output

R-2R

Utilizes current dividers

And many more

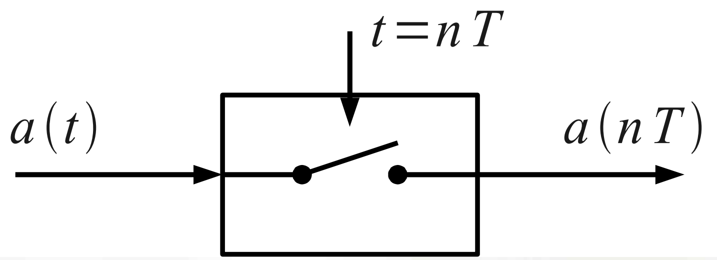
Oversampling DACs, etc.



A/D conversion

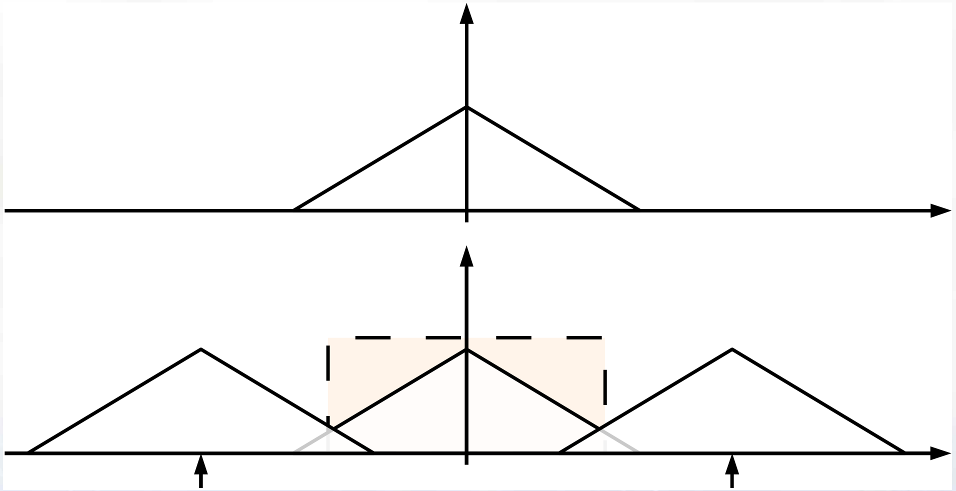
A/D conversion is essentially a sampling process

$$a(nT) = a(t)\big|_{t=nT}$$



Poission's summation formula

$$A\left(e^{j\omega T}\right) = \sum A\left(j\left(\omega - 2\pi k\right)\cdot T\right)$$



Spectrum might repeat and overlap itself!

A/D conversion, cont'd

To avoid folding:

- meet the sampling theorem (theoretically minimizes error)
- use an anti-aliasing filter (practically minimizes error)

Practically, an amount of oversampling is required to meet the tough filter requirements

Analog input is mapped to a digital code

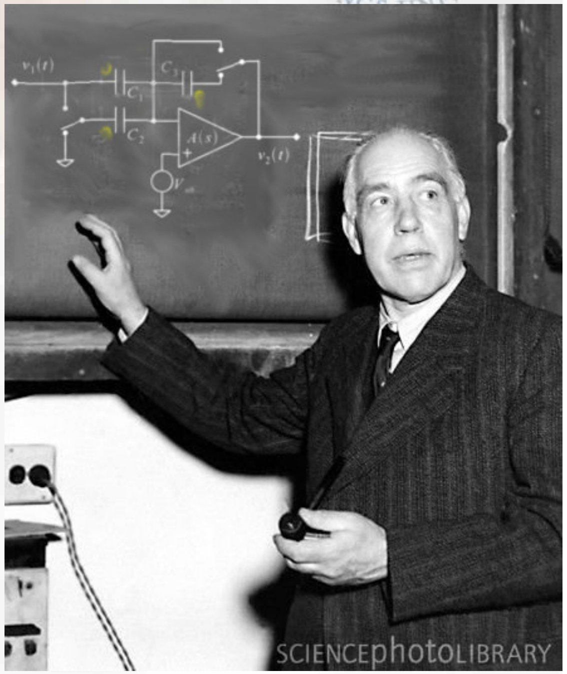
- A range of the input mapped to a unique digital code

$$D(nT) = \sum_{k=0}^{N-1} w_k(nT) \cdot 2^k$$

A/D converter architectures

Flash

A set of comparator measures the input and compares it with a set of references.



Sub-ranging

Use a coarse stage to quantize the input. Subtract the input from the reconstructed, quantized result, amplify it and quantize again.

Pipelined

A set of sub-ranging ADCs

Successive approximation

One sub-ranging ADCs looping in time rather than a straight pipeline.

And plenty of others

Slope, dual-slope, folding, Oversampling ADCs later today

Data converter errors, DNL

Differential nonlinearity is the deviations from the desired steps

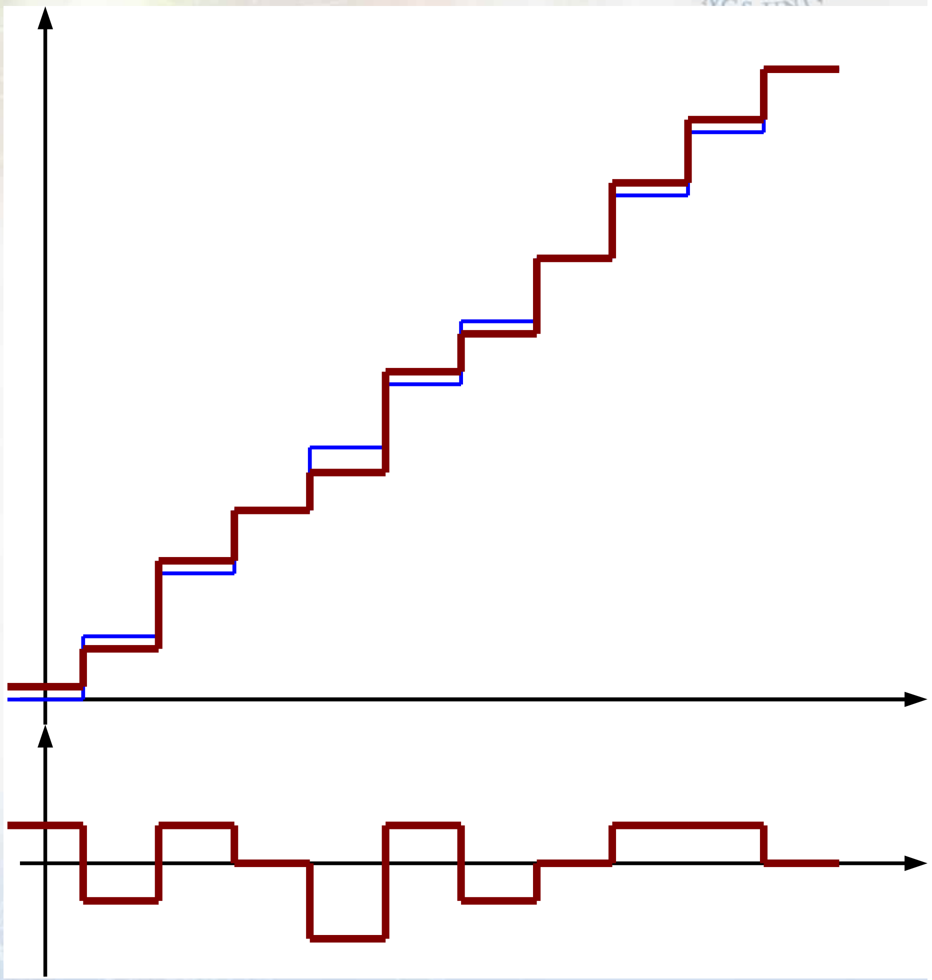
$$\mathrm{DNL}(n)=C_n-C_{n-1}-\Delta$$

or

$$\mathrm{DNL}(n)=\frac{C_n-C_{n-1}}{\Delta}-1$$ [LSB]

For full accuracy

$$|\mathrm{DNL}(n)|<0.5\ \mathrm{LSB}\quad \forall n$$



Often, the gain and offset errors are eliminated from the expression.

Data converter errors, INL

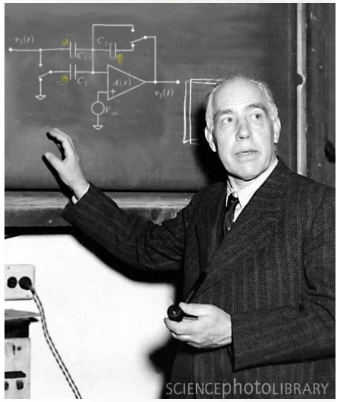
Integral nonlinearity is the deviation from the desired "line"

$\mathrm{INL}(n) = C_n - n \cdot \Delta$ or $\mathrm{INL}(n) = \frac{C_n}{\Delta} - 1$ [LSB]

For full accuracy

$$|\mathrm{INL}(n)| < 1 \ \mathrm{LSB} \quad \forall n$$

One can also show that the INL is the sum of the DNL



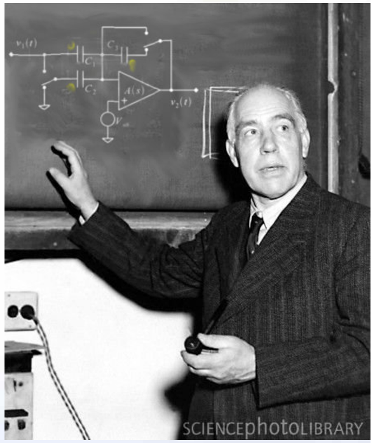
Data converter errors, relations

Static measures

- INL, DNL
- Gain, offset

Dynamic measures

- Spurious-free dynamic range, SFDR
- Signal-to-noise-and-distortion ratio, SNDR
- Intermodulation distortion, IMD
- Resolution bandwidth
- Effective number of bits
- Glitches



Linearity errors are signal dependent!

Typical causes of static errors

Mismatch in reference levels

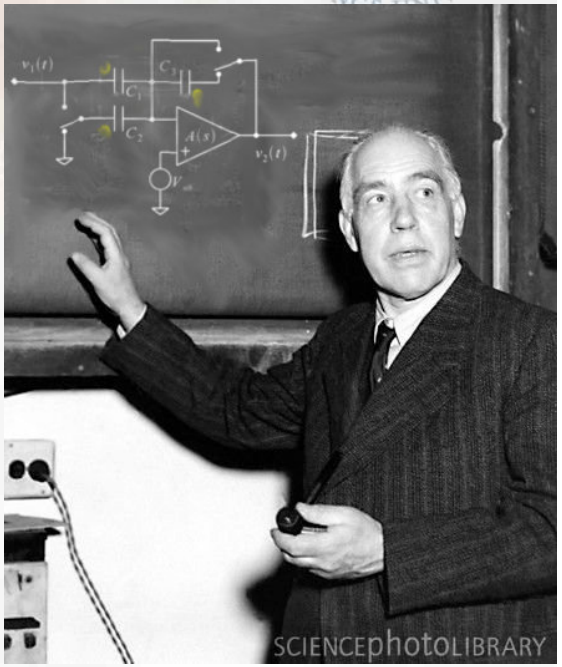
- The effective resistor sizes or currents might vary due to mismatch

Offset in comparators

- Any "modern" continuous-time amplifier has signficant offset

Nonlinear effects due to unmatched biasing

- A power rail will introduce a gradient which will give a nonlinear transfer



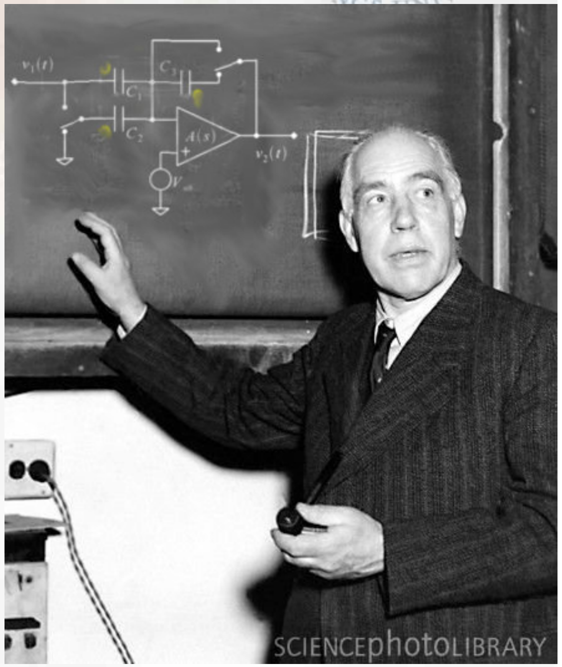
Ways to circumvent the errors

Coding schemes in DACs

- Thermometer vs binary
- Effects with respect to mismatch
- A first glance at a scrambling technique

Digital error correction in pipelined ADCs

- Revisited later



Converter trade-offs, speed vs resolution

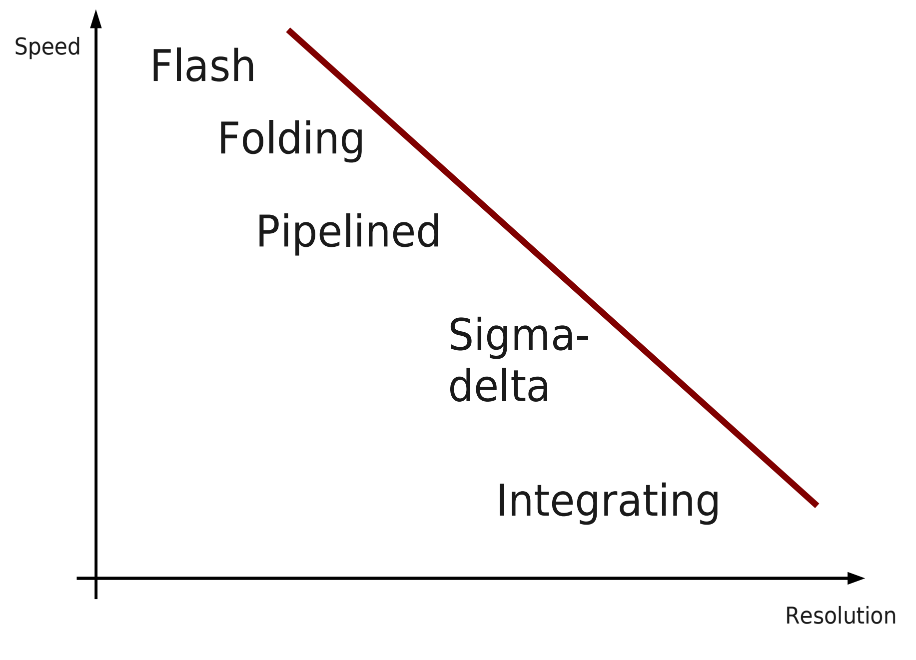
A common figure-of-merit:

$$\mathrm{FOM} = \frac{4kT \cdot f_{bw} \cdot \mathrm{DR}}{P}$$

Some conclusions from this formula

High-speed converters cost power

High-resolution converters cost area



What did we do today?

Data converter fundamentals

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- ADCs
- Transfer characteristics
- Error measures
- Typical architectures

What will we do next time?

Data converter

- Sigma-delta modulators

- Some extras

Wrap-up