Lecture 2, Amplifiers 1

Analog building blocks

LiU EXPANDING REALITY

Outline of today's lecture

Further work on the analog building blocks

- Common-source, common-drain, common-gate
- Active vs passive load

Other "simple" analog building blocks

- Current mirrors

Mismatch

- And other things related to that

What did we do until now?

Stress on the complexity of analog design.

It is not easy and it will take many years before you master.

Why analog design?

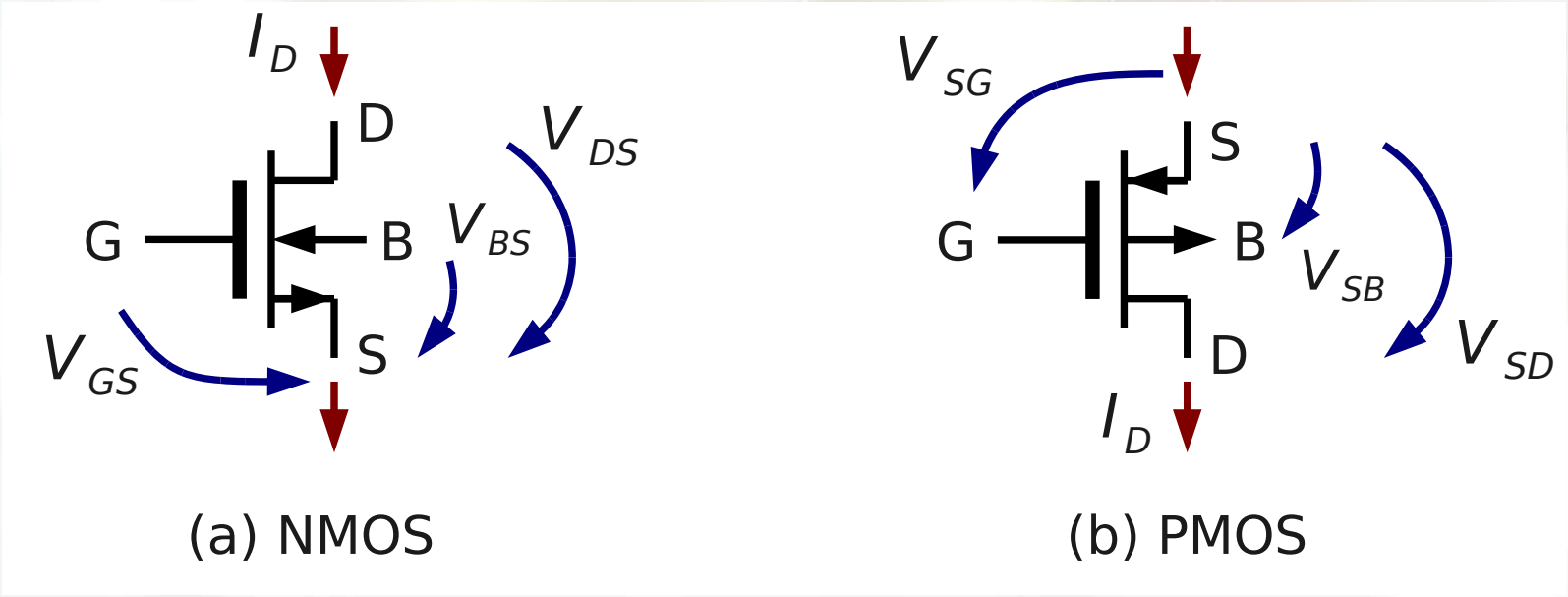
Our world is analog and telecommunication needs analog to interface

Complexity is growing as (n)ever.

Common-source stage and small signal schematics

Operating point vs small-signal schematics and how they "move" around

Transistor, revisited



$$I \approx \alpha V_{eff}^2 \cdot \left(1 + \frac{V_{ds}}{V_\theta}\right)$$

Transistors, small-signal expressions

Linearization gives a small-signal model with these properties:

Expression	Cut-off	Linear	Saturation	
g_m	$\frac{\kappa I_D}{kT/q}$	$2\alpha v_{ds}$	$\frac{2I_D}{v_{eff}}$	$2\sqrt{\alpha I_D}$
g_{mbs}	$g_m \cdot \frac{1-\kappa}{\kappa}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$	
g_{ds}	λI_D	$2\alpha\left(v_{eff}-v_{ds}\right)$	λI_D	

Transistor gain vs region

Using the small-signal parameters gives us the following:

Expression	Cut-off	Linear	Saturation	
$A = \frac{g_m}{g_{ds}}$	$\frac{\kappa \cdot q}{\lambda \cdot k\,T}$	$\frac{v_{ds}}{v_{eff} - v_{ds}}$	$\frac{2}{\lambda \cdot v_{eff}}$	$\frac{2\sqrt{\alpha}}{\lambda\sqrt{I_D}}$

What can you spot (where is the gain highest)?

$\kappa \approx 0.75$ and $k\,T/q \approx 26$ mV.

Poles, bandwidth, gain, etc.

Bode plot

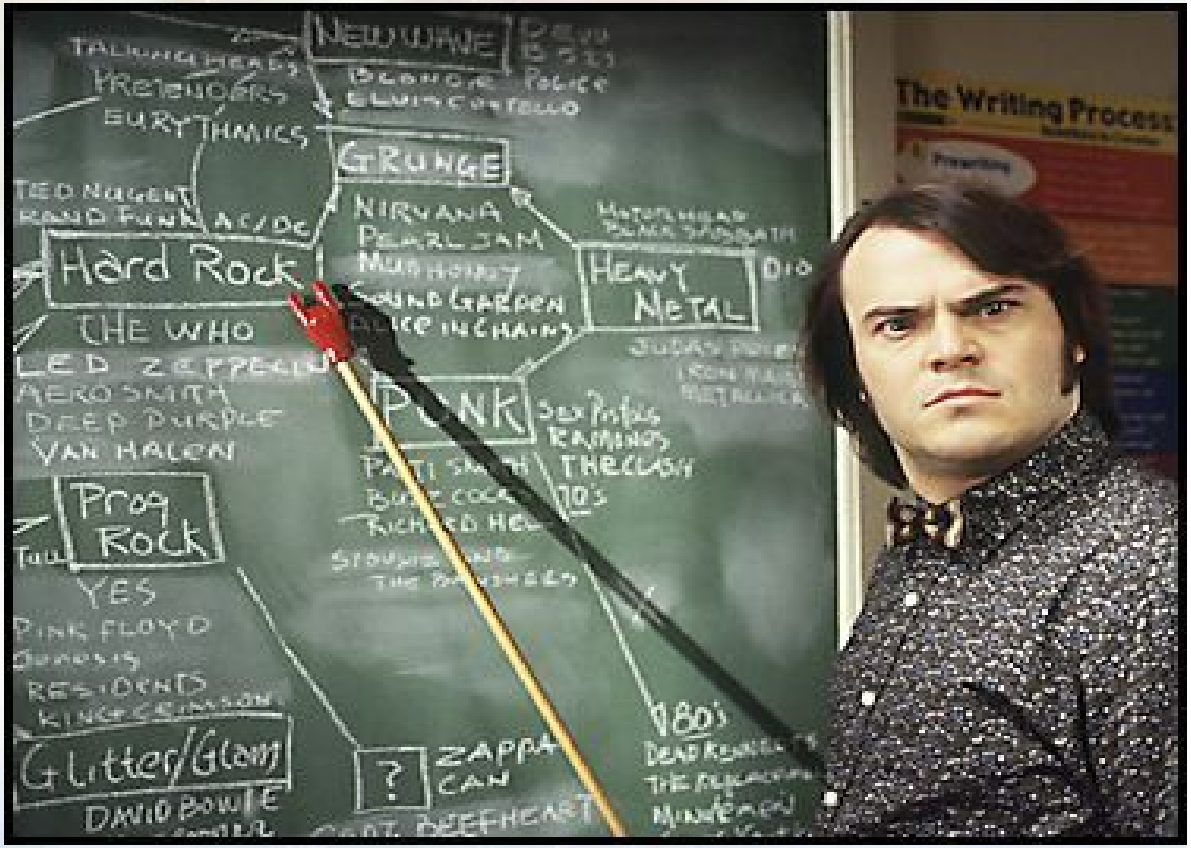
Approximations

Pole vs gain vs unity-gain

Hand-calculations, practical tips

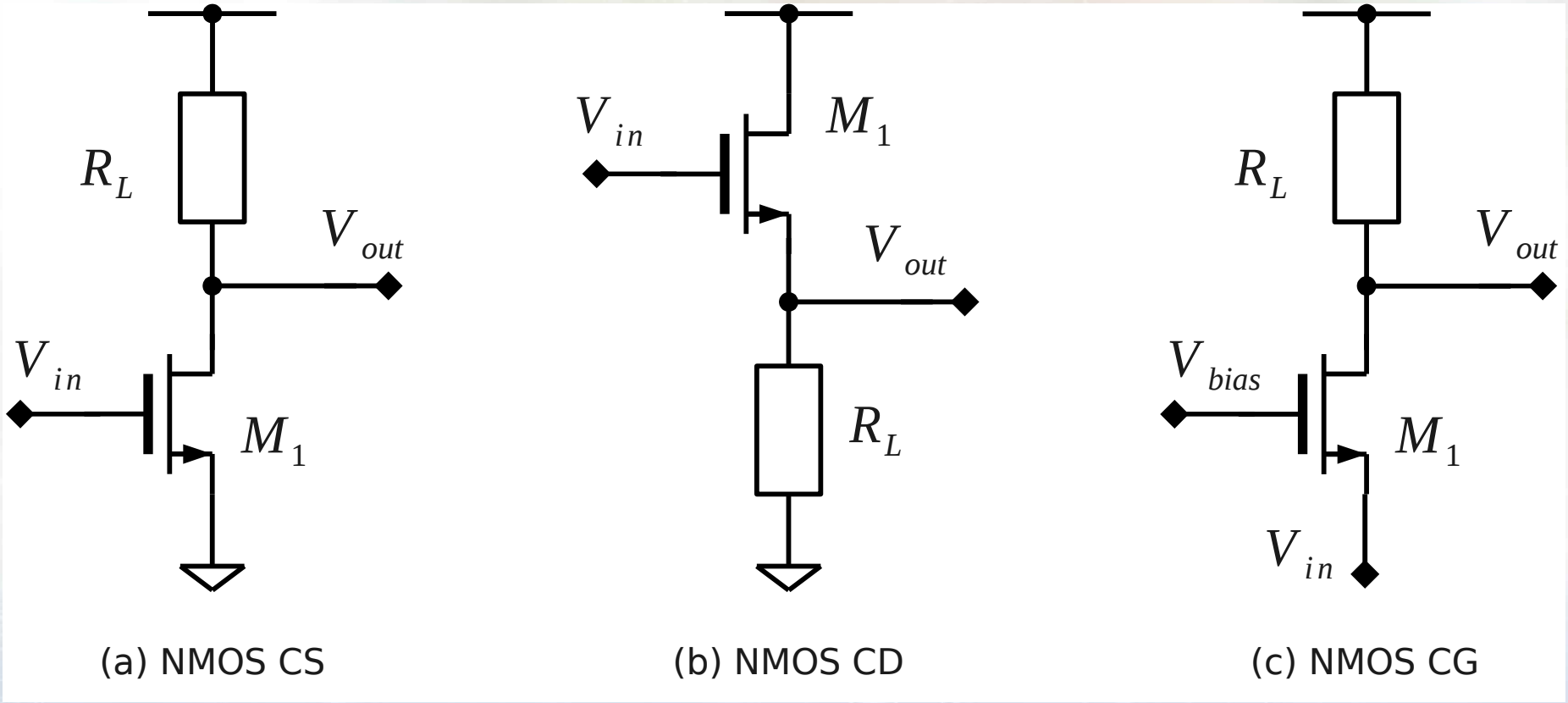
Settling vs pole

Speed



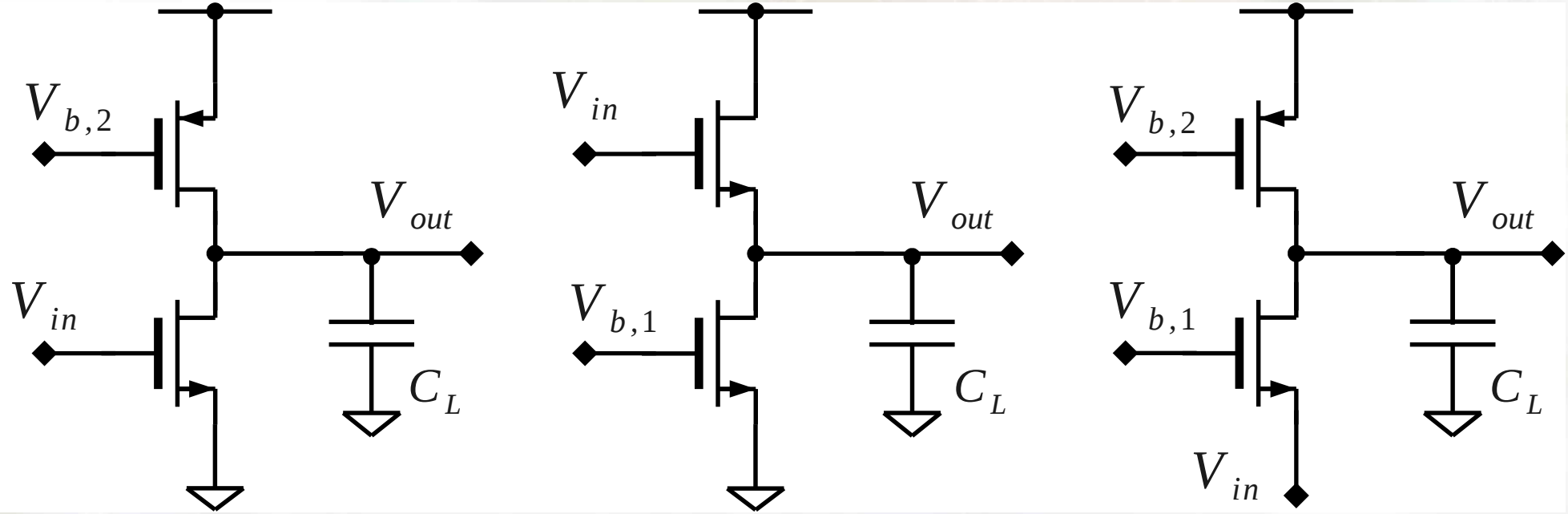
Amplifier stages, passive load

Common-source, common-drain, common-gate



(a) NMOS CS (b) NMOS CD (c) NMOS CG

Amplifier stages, active load



Why active load?

Amplifier stages, compiled 1

Expression	CS	CD	CG*)
DC gain, $A_0 \approx \frac{g_m}{g_{out}}$	$\approx \frac{g_m}{g_P + g_N}$	$\approx \frac{g_m}{g_m + g_P + g_N} \approx 1$	$\approx \frac{g_m}{g_P + g_N}$
Output impedance, $\approx g_{out}$	$\approx g_P + g_N$	$\approx g_m$	$\approx g_P + g_N$
Bandwidth, $p_1 \approx \frac{g_{out}}{C_L}$	$\approx \frac{g_P + g_N}{C_L}$	$\approx \frac{g_m}{C_L}$	$\approx \frac{g_P + g_N}{C_L}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx g_m / C_L$	N/A (why?)	$\approx g_m / C_L$

Source impedance not mentioned, see exercises.

Amplifier stages, compiled 2

Expression	CS	CD	CG*)
DC gain, $A_0 \approx g_m / g_{out}$	$\approx 1/\lambda \cdot v_{eff}$	≈ 1	$\approx 1/\lambda \cdot v_{eff}$
Output impedance, $\approx g_{out}$	$\approx \lambda I_D$	$\approx 2 I_D / v_{eff}$	$\approx \lambda I_D$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \lambda I_D / C_L$	$\approx 2 I_D / C_L \cdot v_{eff}$	$\approx \lambda I_D / C_L \cdot v_{eff}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx I_D / C_L \cdot v_{eff}$	N/A (why?)	$\approx I_D / C_L \cdot v_{eff}$

Voltage swings

Walk around the circuit

Check for all the required voltage levels to maintain transistors in their saturation region

Use the following relations

$$V_{GS} = V_{EFF} + V_T, \quad V_{DS} > V_{EFF} \Rightarrow V_{DS} = V_{EFF}, \quad V_{EFF} = \sqrt{\frac{I_D}{\alpha}}$$

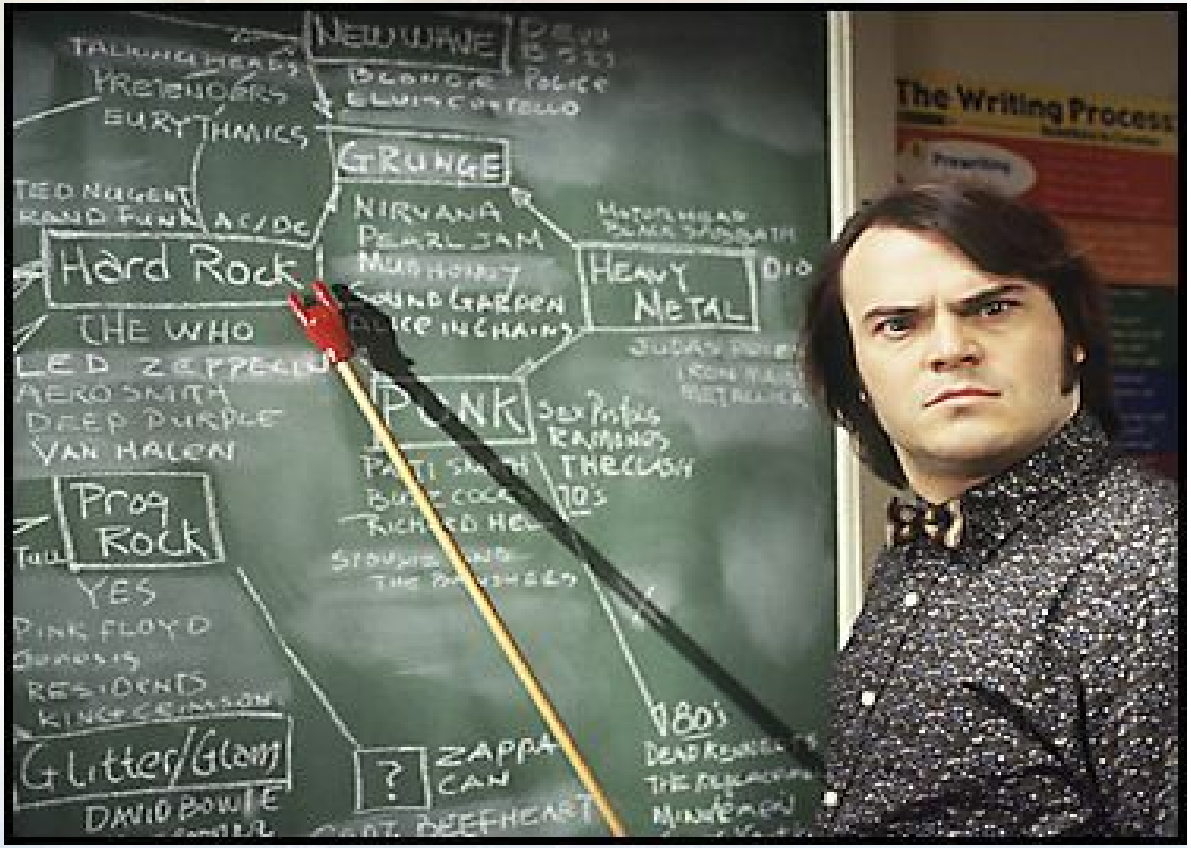
The lower v_{eff}, the ...

higher swing

higher gain

Examples

Consider the three amplifiers and check the potentials



Some other relationships

Expression	Generic	CG/CS	CD
Slew rate	$\mathrm{SR} \approx \frac{I_D}{C_L}$	$\approx \omega_u \cdot v_{eff}$	$\approx \frac{p_1 \cdot v_{eff}}{2}$
Noise, input-referred	$v_n^2(f) \approx \frac{4kT\gamma}{g_m}$	$\approx \frac{2kT\gamma \cdot v_{eff}}{I_D}$	
Noise, total output	$v_{out}^2 \approx \frac{kT\gamma A_0}{C_L}$	$\approx \frac{kT\gamma}{\lambda C_L v_{eff}}$	$\approx \frac{kT\gamma}{C_L}$

Mismatch, or

"In reality, nothing is perfect ..."

Differences in

- Fabs (wafer-to-wafer, fabrication, date)
- Wafer locations (chip-to-chip, doping)
- Transistor (block-by-block, orientation and side effects, doping)
- Temperatures, Voltages, Currents

You cannot assume that one transistor is identical to another

- Especially not for high-speed, high-accuracy applications

Mismatch, cont'd

The drain current in the saturation region:

$$\Delta I_D = \underbrace{\frac{dI_D}{d\beta}\cdot\Delta\beta + \frac{dI_D}{dS}\cdot\Delta S}_{\Delta\alpha} + \frac{dI_D}{dV_{eff}}\cdot\Delta V_{eff} + \frac{dI_D}{dV_{ds}}\cdot\Delta V_{ds} =$$

$$= \underbrace{\frac{I_D}{\beta}\cdot\Delta\beta + \frac{I_D}{S}\cdot\Delta S}_{\Delta\alpha} + \frac{2I_d}{V_{eff}}\cdot\Delta V_{eff} + \frac{\lambda I_d}{1+\lambda(V_{ds}-V_{eff})}\cdot\Delta V_{ds} \Rightarrow$$

$$\frac{\Delta I_D}{I_D} = \underbrace{\frac{\Delta\beta}{\beta} + \frac{\Delta S}{S}}_{\Delta\alpha} + \frac{2\Delta V_{eff}}{V_{eff}} + \frac{\lambda\Delta V_{ds}}{1+\lambda(V_{ds}-V_{eff})} \Rightarrow$$

$$\frac{\Delta I_D}{I_D} \approx \frac{\Delta\alpha}{\alpha} + \frac{2\Delta V_{eff}}{V_{eff}}$$

Mismatch, cont'd

Ignoring the low-impact ones, and assuming that they are decoupled, gives us, with the help of stochastic variables:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right)=\sigma^2\left(\frac{\Delta \alpha}{\alpha}\right)+\frac{\sigma^2\left(\Delta V_{eff}\right)}{V_{eff}^2}$$

First-order assumptions

$$\sigma^2\left(\frac{\Delta \alpha}{\alpha}\right)\approx\frac{A_S^2}{W\cdot L}$$ and $$\sigma^2\left(\Delta V_{eff}\right)\approx\frac{A_{VT}^2}{W\cdot L}$$

Second-order assumptions

Distance-related, correlations, etc.

Current mirrors

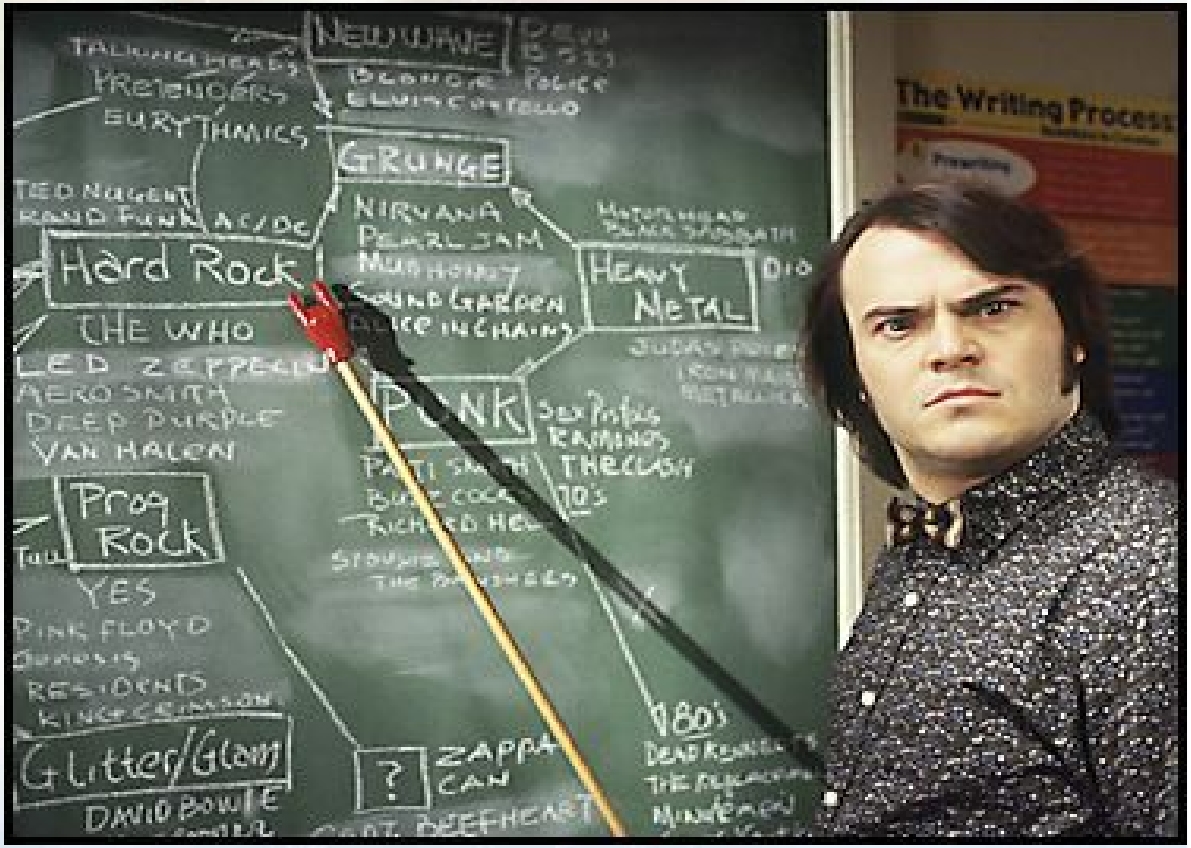
Distribute currents

Set bias levels

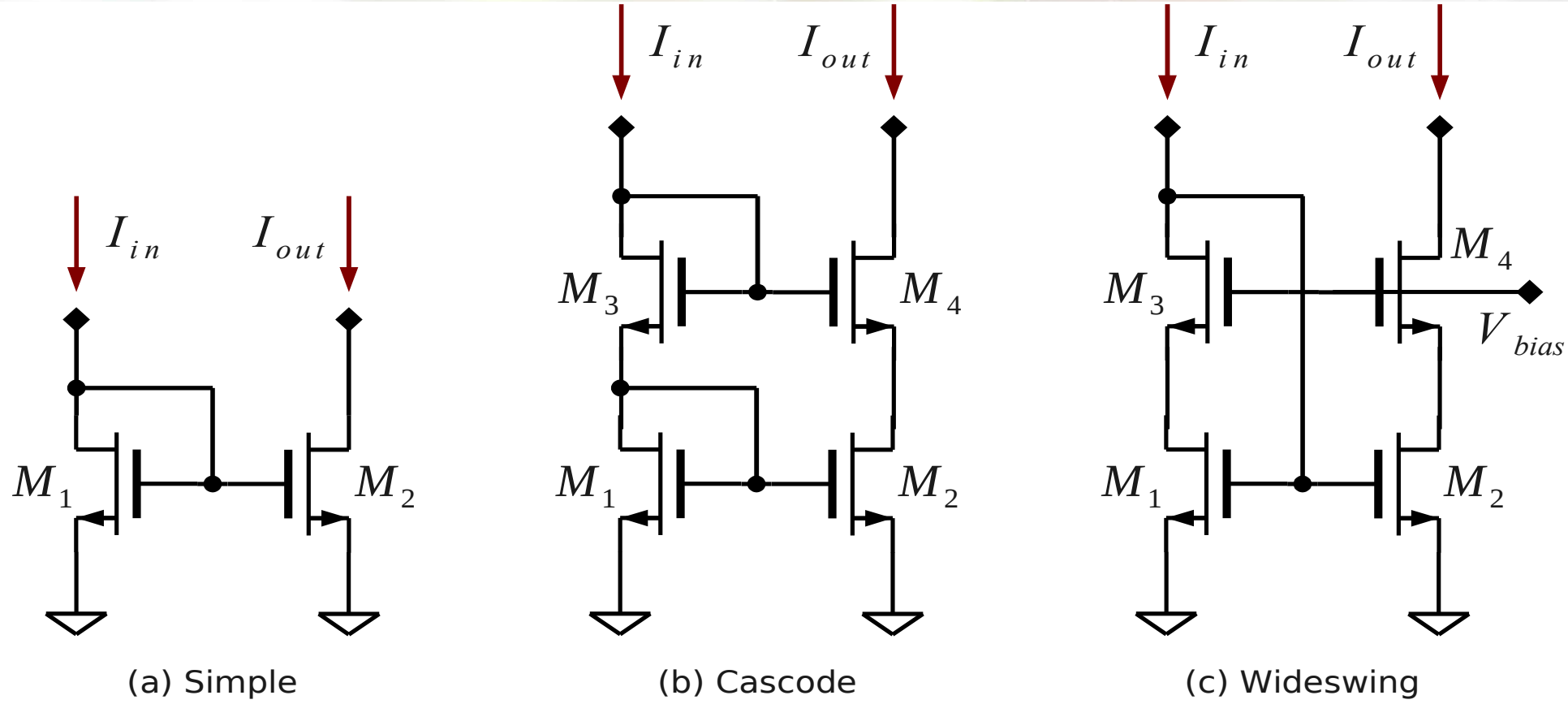
"Equal" current through many branches

Decouple design parameters

Gain is now controlled by current instead



Current mirrors, cont'd

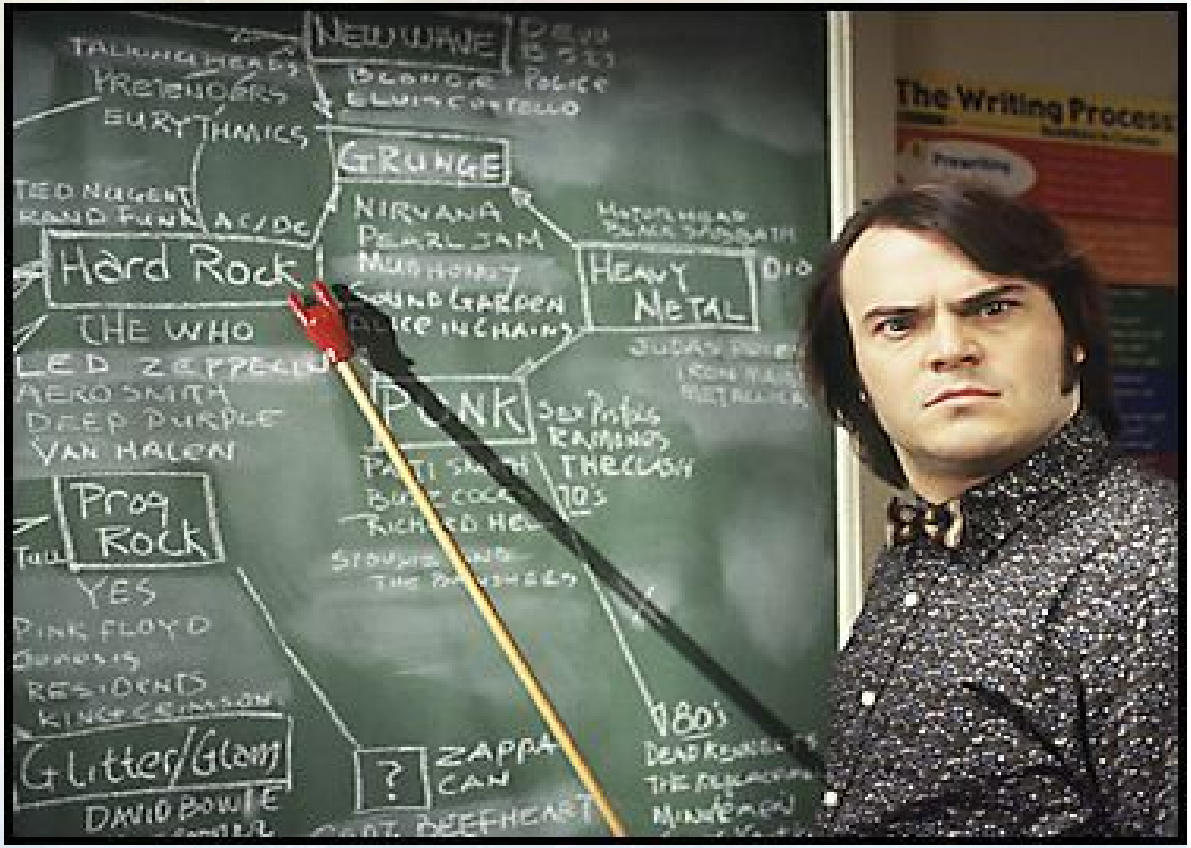


Current mirrors, some maths

Swing

Input impedance

Output impedance



What did we do today?

Went through the other important CMOS building blocks

CG, CD, CS, (CI)

Current mirrors

How to bias a circuit (current mirrors)

Pros and cons with different current mirrors

Mismatch

What will we do next time?

Amplifiers and differential pairs

Why differential?

Stability

Why stability?

Phase margin

Compensation