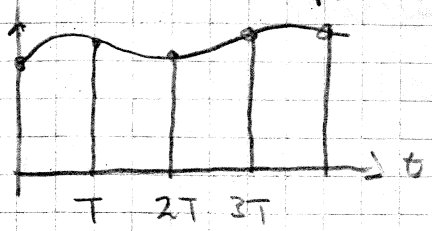
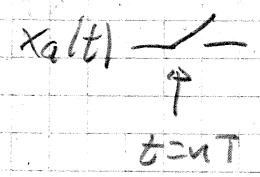
Fö Data converters

A/D-conversion: Uniform sampling and amplitude quantization.

Uniform sampling

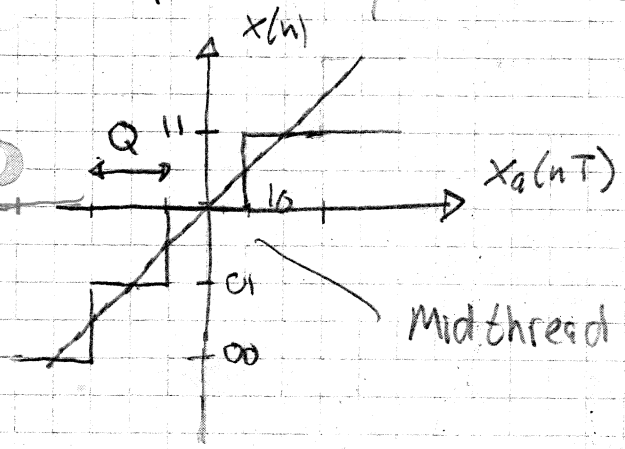


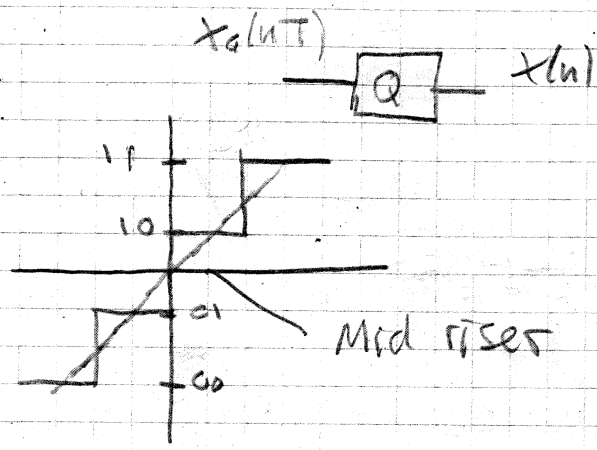


$f_s = \frac{1}{T}$ sampling frequency $\quad f_s > 2B$

B signal bandwid

Amplitude quantization





Quantization step Q

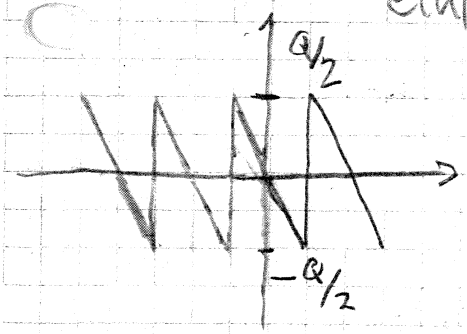
$Q = \frac{V_{range}}{2^N}$, V_{range} is quantized input range

N is the resolution ie number of bits

Quantization error

$e(n) = x(n) - x_q(nT) =$

$= [x_a(nT)]_Q - x_q(nT)$



e(n) is often modelled as an uncorrelated zero-mean noise source with variance (power) $\sigma_e^2 = \frac{Q^2}{12} = \frac{V_{range}^2 \cdot 2^{-2N}}{12}$

$SNR = 10 \cdot \log_{10}\left[\frac{P_{signal}}{P_{noise}}\right]$ = / full swing sinusoid /

$= 6{,}02N + 1{,}76$

$$SNDR = 10 \cdot \log_{10}\left[\frac{P_{signal}}{P_{noise+P_{distortion}}}\right]$$

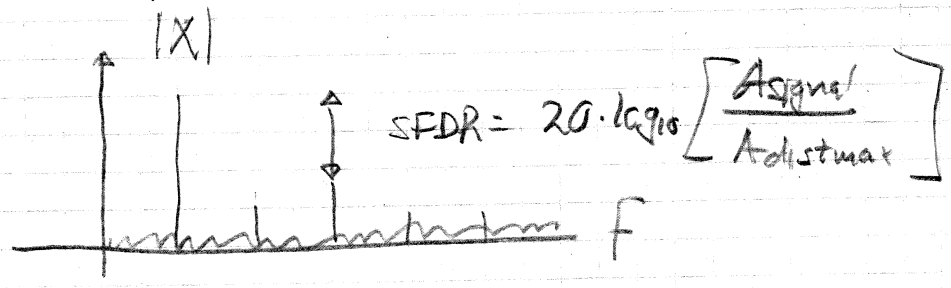
(SINAD)

Effective resolution

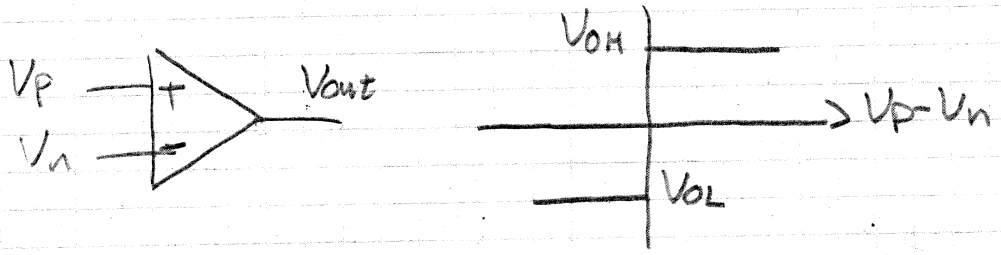
$$ENOB = \frac{SNDR - 1,76}{6,02}$$

Ex:) Accuracy (N): 14 bits
Resolution 12,1 bits

SFDR



Comparators

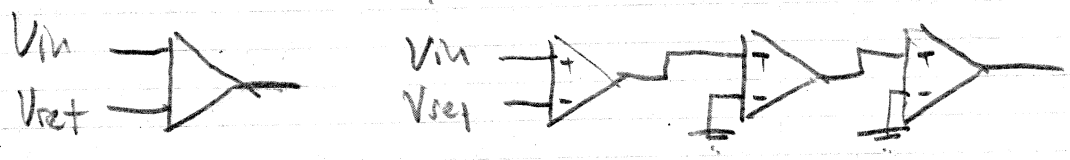


Vp is compared with Vn. Used to realize the signal quantization.

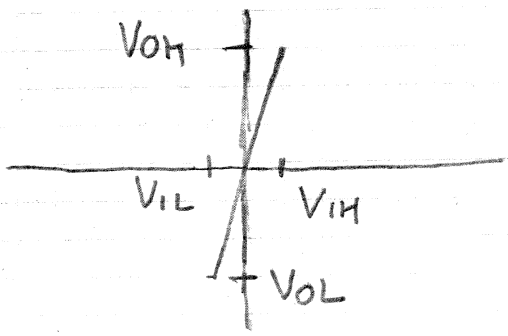
Two types

1) Single or multistage open-loop amplifiers
2) Regenerative comparators (Latched comparators)

Open-loop amplifier comparators



Finite gain



With a finite gain there will be a minimum input signal that can be resolved

High gain is desireable

Characteristic resolution parameter

C_F is the smallest input signal that can be compared

$$[V_{OH} - V_{OL}] = A_v [V_{IH} - V_{IL}]$$

$$C_F = \frac{[V_{OH} - V_{OL}]}{A_v}$$

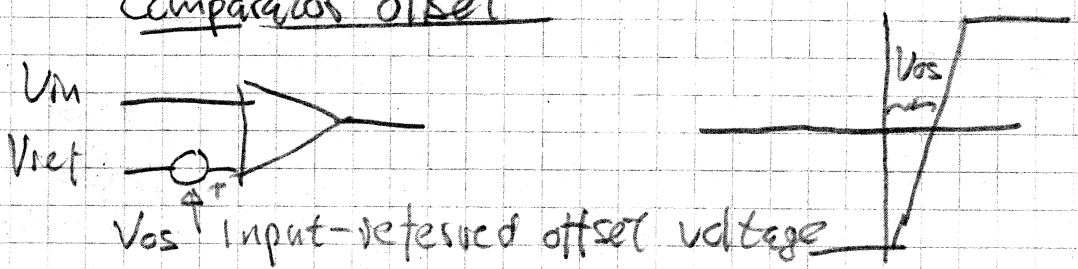
Example ADC input voltage range 1 V, $N = 10 \Rightarrow$

$$LSB = Q = \frac{1}{2^{10}} = 0{,}98\,mV$$

$$V_{IH} - V_{IL} \leq 0{,}98\,mV \Rightarrow A_v > \frac{V_{OH} - V_{OL}}{[V_{IH} - V_{IL}]_{min}} = \frac{3}{0{,}98\,mV} =$$

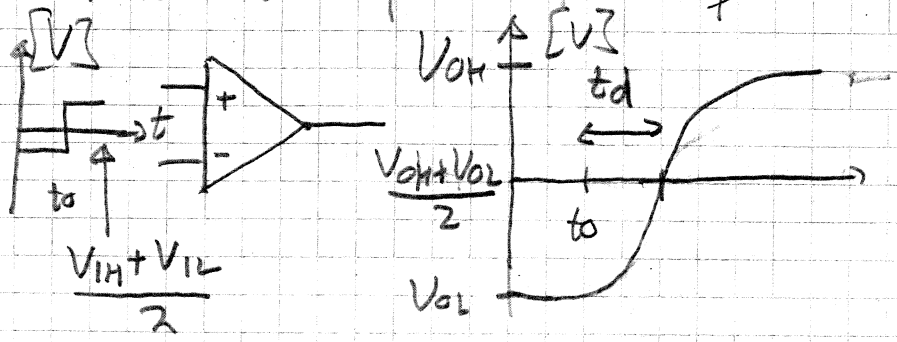
$$= 3072 \leftrightarrow 69{,}8\ dB$$

Comparators offset



Comparators propagation delay td

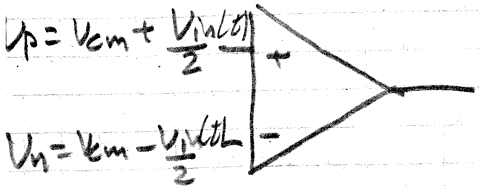
- Limits the speed of a quantizer (ADC)



$$td = t\left[V_{out} = \frac{V_{OH} + V_{OL}}{2}\right] - t\left[V_{in} = \frac{V_{IH} + V_{IL}}{2}\right]$$

Example Comparator Speed-Accuracy Trade-off

The larger the input step size the shorter the propagation delay. How is the delay related to accuracy?

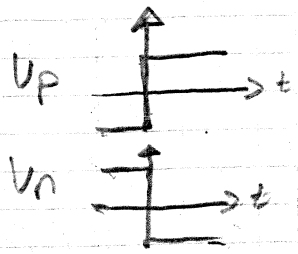


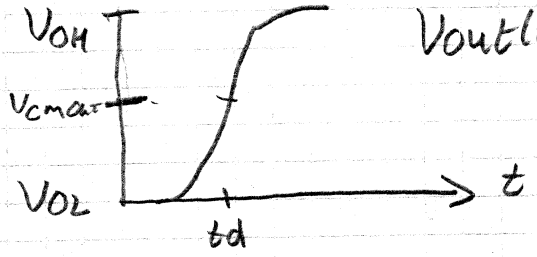
Single-pole model

$$H(s) = \frac{A_0}{1 + s/\omega_c}$$

$V_{in}(t) = V_{step} \cdot u(t) \Rightarrow \ldots$

$$V_{out}(t) = V_{step} A_0 \left[1 - e^{-\omega_c t}\right] u(t)$$





Apply the min. inp. voltage $V_{step} = V_{in,min} = V_{IH} - V_{IL} = \frac{V_{OH} - V_{OL}}{A_0}$ as step size. The comparator output at $t = t_d$:

$$V_{out,total}(t_d) = \frac{V_{OH} + V_{OL}}{2} = V_{OL} + \underbrace{\left[V_{OH} - V_{OL}\right]}_{A_0} A_0 \left[1 - e^{-\omega_c t_d}\right]$$

(V_{OL} = V_{DC}; A_0 = V_{step})

$$\Rightarrow \frac{1}{2} = 1 - e^{-\omega_c t_d}$$

$$t_d = \frac{1}{\omega_c} \cdot \ln(2)$$ Min input step applied $\Rightarrow$

$$t_{d,max} = \frac{1}{\omega_c} \ln(2)$$

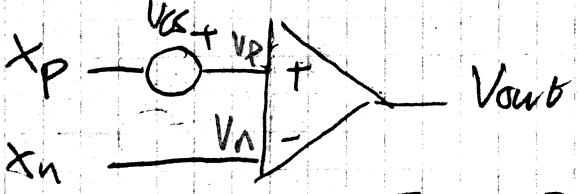
A larger step $V_{step} = k \cdot V_{in,min} \Rightarrow$ $k \geq 1$

$$t_d = \frac{1}{\omega_c} \ln\left[\frac{1}{1 - \frac{1}{2^k}}\right]$$

Hence, the larger the input signal (lower resolution) the shorter propagation delay

Speed- accuracy trade-off

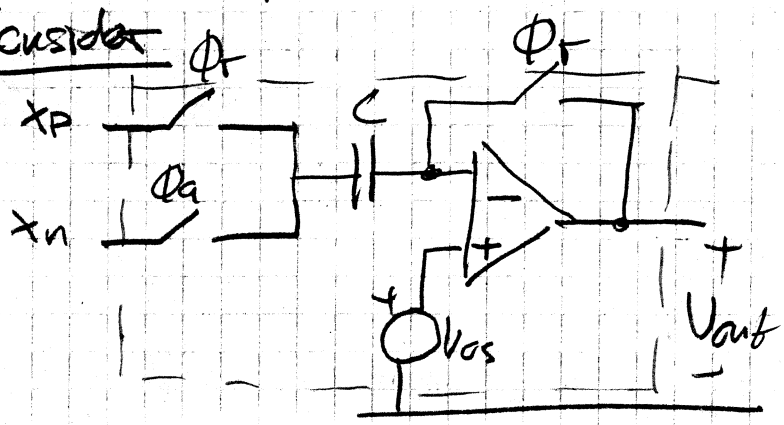
Comparator Offset Voltage compensation by dynamic biasing



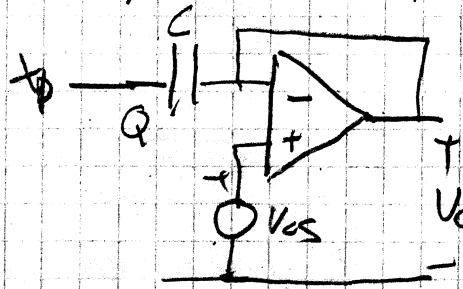
$$V_{out} = A[V_p - V_n] = A[x_p + V_{os} - x_n] =$$

$$A[x_p - x_n] + A V_{os}$$

Consider



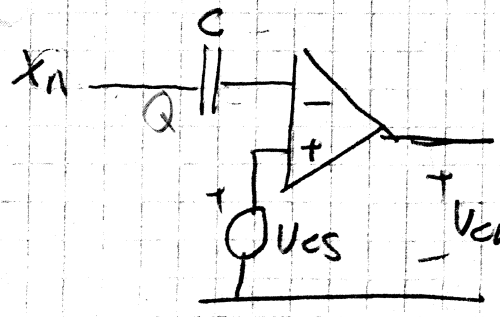
$t = t_0$, Φ_t closed, Φ_a open



$V_{out} = V_n = A[V_{os} - V_n]$, $V_n = \frac{A}{1+A} V_{os}$

$$Q(t_0) = C\left[x_p(t_0) - V_n(t_0)\right] = C\left[x_p(t_0) - \frac{A}{1+A} V_{os}\right]$$

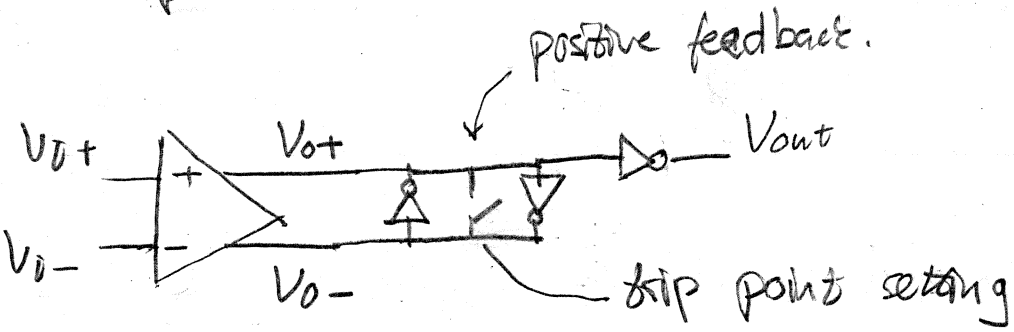
$t = t_1$, Φ_t open, Φ_a closed



$$Q(t_1) = C\left[x_n(t_1) - V_{os} + \frac{V_{out}(t_1)}{A}\right] = Q(t_0) \Rightarrow$$

$$V_{out}(t_1) = A[x_p(t_0) - x_n(t_1)] + A V_{os} \cdot \underbrace{\left[\frac{1}{1+A}\right]}_{\text{small !}}$$

Regenerative Comparators (latched)



Any imbalance $\Delta V_0 = V_{0+} - V_{0-}$ will regenerate V_{out} quickly towards V_{DD} or V_{SS}.
The comparison starts when the trip point switch is opened.

Metastability

If the comparator output has not reached a valid logical voltage level within the conversion period T, the comparator is said to have entered a metastable state.

P(Metast. state) and Mean time to failure MTF

The reliability of a latched comparator is measured by the MTF.

For a flip-flop: $P(t_{comp} > \frac{T}{2}) \approx e^{-\frac{(A_0-1)}{R_{out}C_L}\cdot\frac{T}{2}}$

where A_0 = comparator gain

R_{out} = inverter output resistance

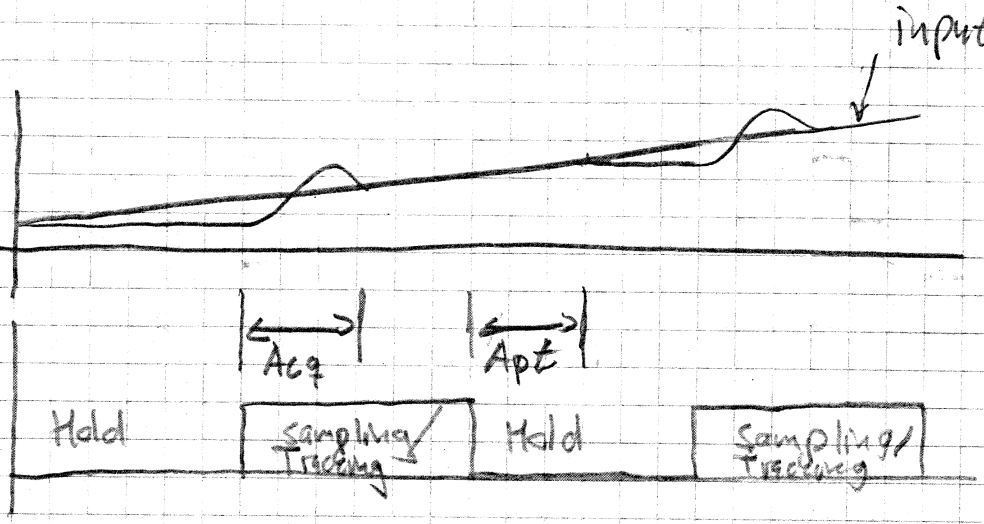
C_L = inverter output load

$$MTF \approx \frac{1}{f_s\, P(t_{comp} > \frac{T}{2})} = \frac{e^{\frac{(A_0-1)}{R_{out}C_L}\cdot\frac{T}{2}}}{f_s} = \left/ \frac{1}{R_{out}C_L} = 2\pi f_{-3dB} \right/ = \frac{2\pi f_t}{A_0}$$

$$= \frac{e^{(1-\frac{1}{A_0})\frac{f_t}{f_s}\pi}}{f_s}$$

Ex | $f_u = 800\ MHz$
$f_s = 80\ MSps$
$A_0 = 100$
$MTF \approx 402 \cdot 10^3\ s = 112\ h$

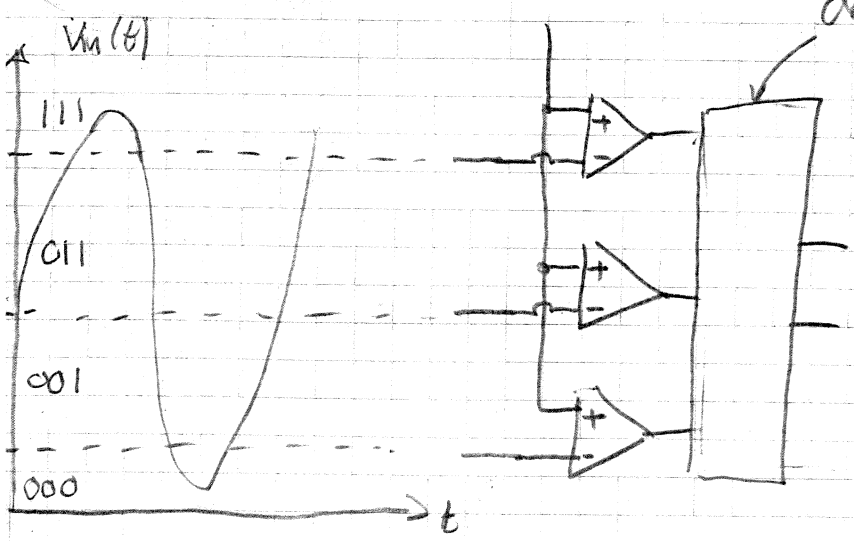
Sample and hold circuits



Acq = Acquisition time
Apt = Aperture time

Acquisition time sets the maximum sampling frequency and is determined by the bandwidth and slewing of the S&H amplifier

Flash ADC

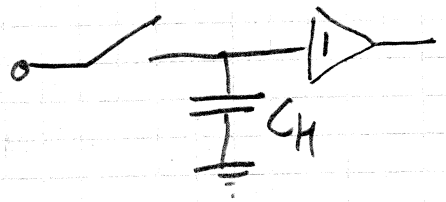


(signal dependent)

Different "ramp slopes" ⇒ different comparator delay ⇒ nonlinear

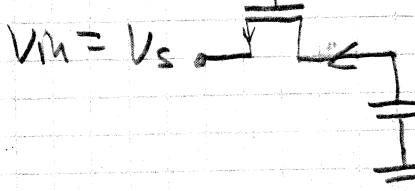
So for resolution > 5-6 bits, S&H is necessary, which holds the input signal to the comparators constant.

Basic S&H



- sampling switch
- Hold capacitor
- Buffer amplifier

NMOS-switch S&H (T&H)



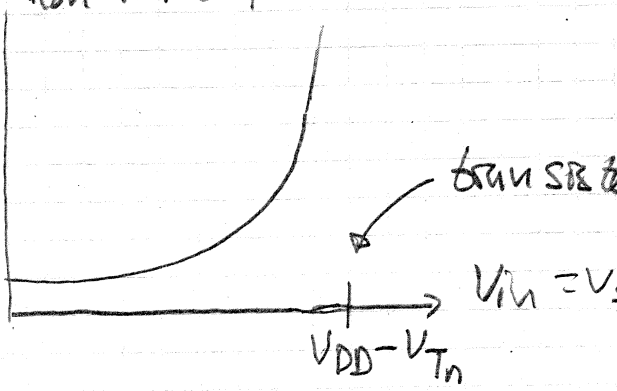
$V_G = V_{DD}$, switch is on, then $V_{DS} < V_{GS} - V_T \Rightarrow$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox}\frac{W}{L}\left[V_{GS}-V_{Tn}-\frac{V_{DS}}{2}\right]} \simeq \text{/ } V_{DS} \text{ small / } \simeq$$

$$\frac{1}{\mu_n C_{ox}\frac{W}{L}\left[V_{DD}-V_{in}-V_T\right]}$$

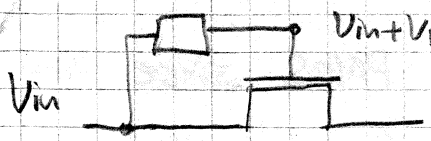
$\therefore$ The on-resistance is signal dependent. $\Rightarrow$ nonlinear distortion



Also, non-zero on-resistance $\Rightarrow$ band limitation

$$V_{out}(s) = \frac{1}{1 + sR_{on}C_H} \cdot V_{in}(s)$$

Boot-strapped sampling switch



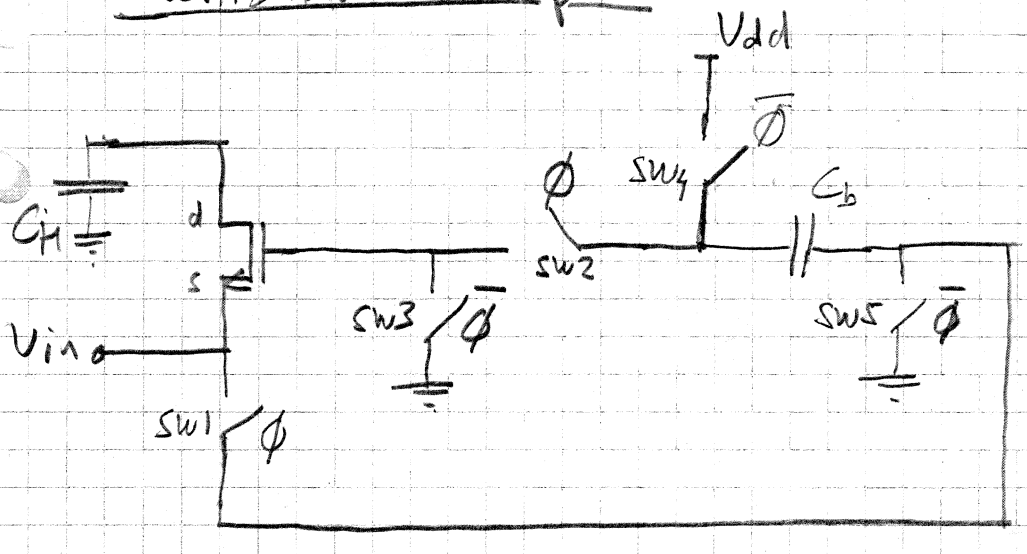
$$R \approx \frac{1}{\beta_n[V_G - V_S - V_T]} = \frac{1}{\beta_n[V_{DD} - V_T]}$$

R becomes more constant. However,

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) = f(V_{SB}) = f(V_{in})$$

The bulk-effect makes R_{on} signal-dependent. (less important than

Realization example

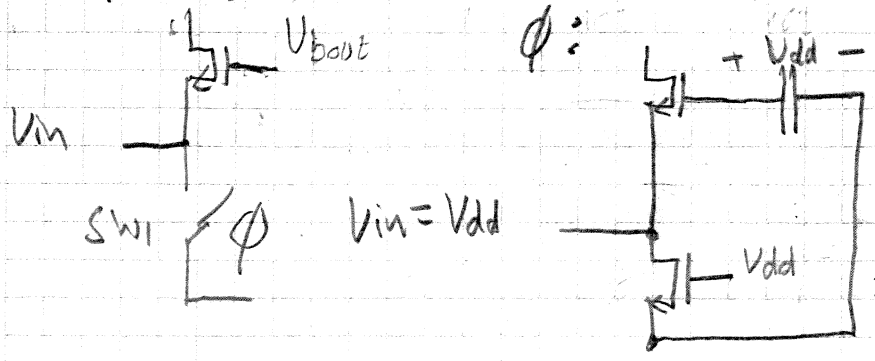


During $\bar{\phi}$: SW1 & 2 are open, SW3 turns switch off and SW4 & 5 charges C_b to V_{dd}

during ϕ V_{dd} is applied between the gate and source of the switch (respectively at $V_S = V_{in}$ through SW 1 & 2.

Main problem: Get the other switches to conduct in rail-to-rail operation

Ex 1)



ϕ:

$V_{gs} = V_{dd} - V_s > V_T \Rightarrow$

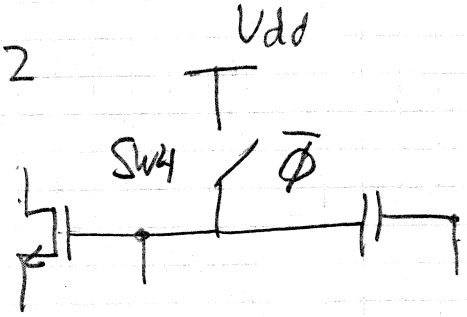
$V_s < V_{dd} - V_T \Rightarrow$

$V_{bootmax} = 2V_{dd} - V_T < 2V_{dd}$

$\Rightarrow V_{inmax}$ for linear operation $= V_{dd} - V_T$

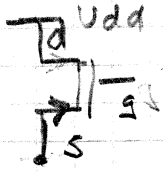
Solution: Tie gate of SW1 to V_{boost}.

Ex 12

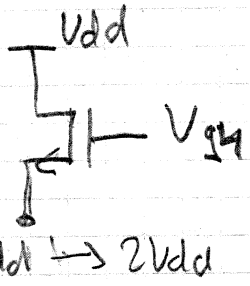


Realization of SW4.

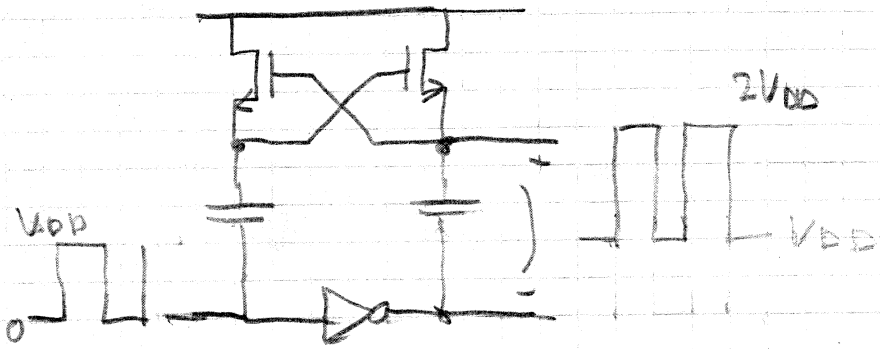
Cannot be PMOS since then it will not be off and hence leak V_{boost}



Then it is NMOS?



Works if V_{SW4} is made to toggle between Vdd and 2Vdd
⇒ Need a charge pump.

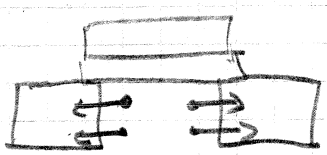


Charge injection

Transistor on

$Q_{CH} \approx WLC_{ox}(V_{GS}-V_T)$

When turning off

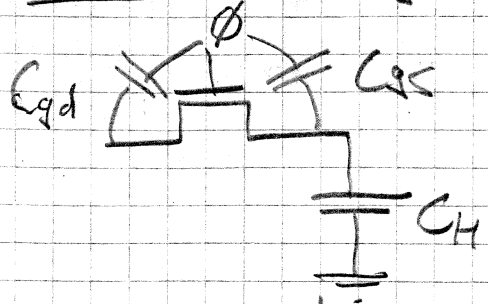


$q_1 + q_2 = Q_{CH}$

Channel charge is pushed into the drain and source.

Charge injected into high-impedance nodes in the signal path causes large errors

Clock feedthrough



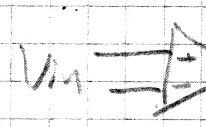
The clock signal is fed into the sampling capacitance node through capacitive coupling

$$\Delta V = \frac{\frac{1}{sC_H}}{\frac{1}{sC_H}+\frac{1}{sC_{gs}}} V_{clk} = \frac{C_{gs}}{C_{gs}+C_H} V_{clk}$$

An amplifier is needed to isolate C_H from the output. The amplifier must be as fast and linear as the sampling switch.

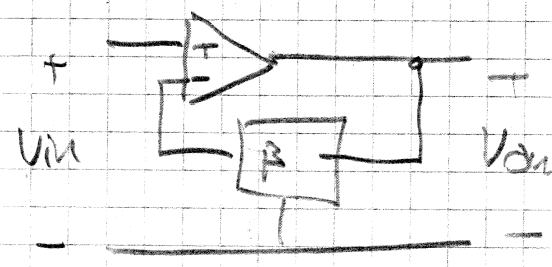
Feedback is always used.

Amplifier without feedback



$$V_{out} = A_v \cdot V_{in} + \underbrace{V_d}_{\text{Distortion}}$$

Amplifier with feedback



$$V_{out} = A_v(V_{in} - \beta V_{out}) + \underbrace{V_d}$$

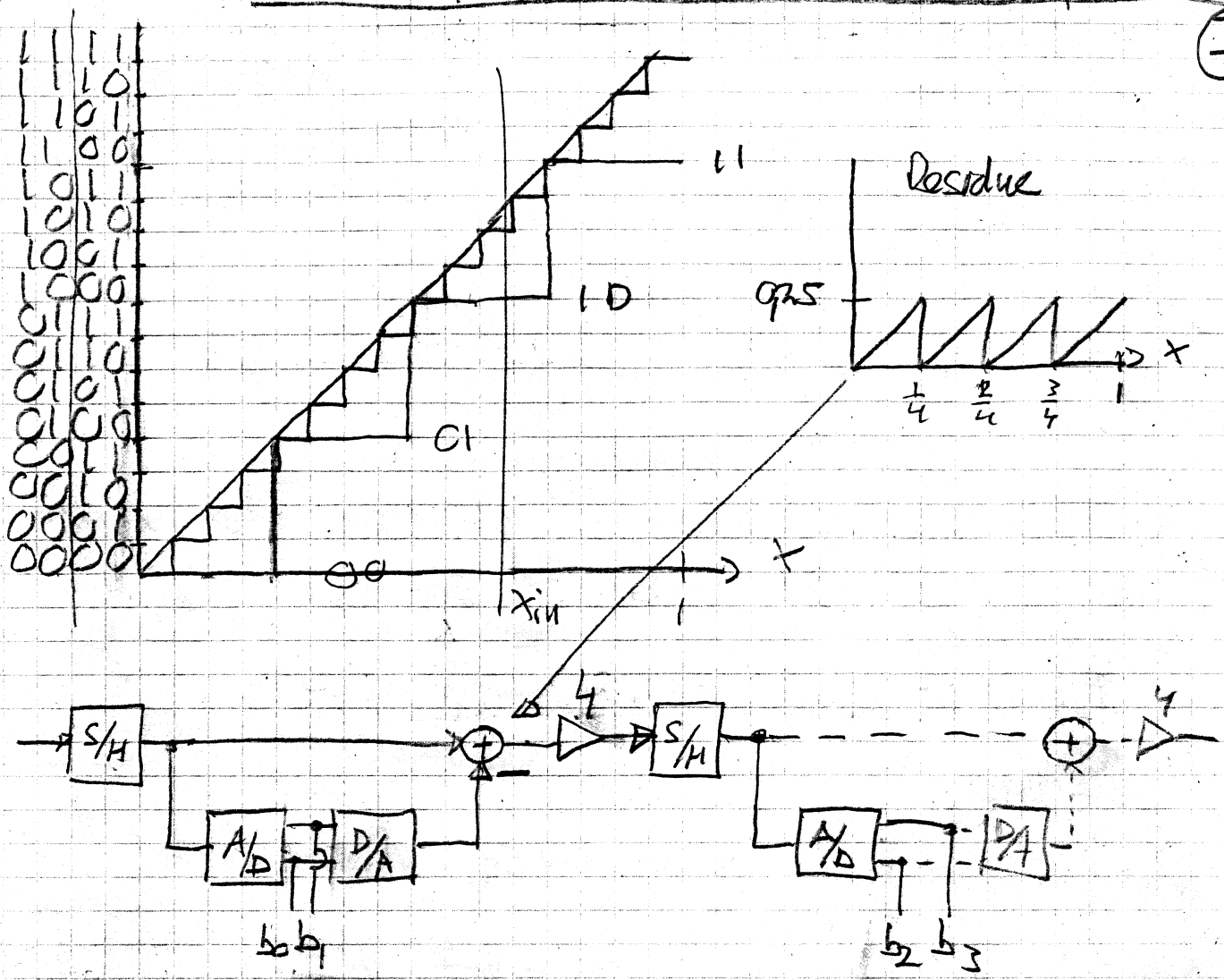
Same distortion for the same output V_{out}.

$$\Rightarrow V_{out}[1+\beta] = A_v V_{in} + V_d$$

$$V_{out} = \underbrace{\frac{A_v}{1+\beta A_v}}\ V_{in} + \underbrace{\frac{1}{1+\beta A_v}}\ V_d$$

Distortion suppressed by $\frac{1}{1+\beta A_v}$

How do we decrease the number of comparators?



This is called a Pipeline ADC

With K N-bit stages

it requires only $K(2^N-1)$ instead of $2^{K \cdot N}-1$ comparators

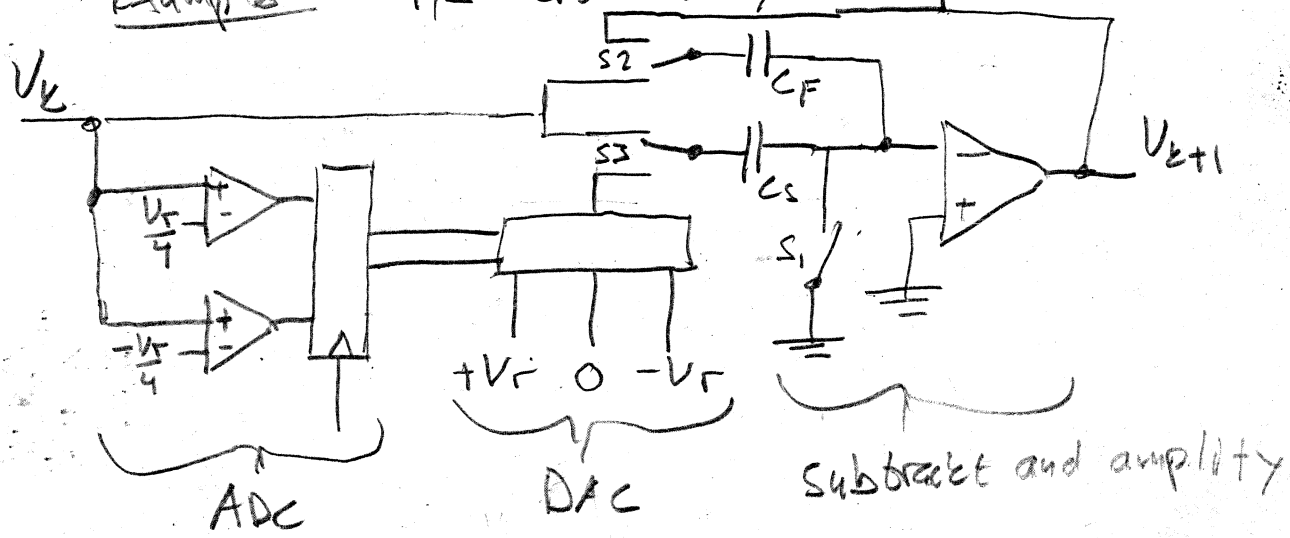
but also K-1 N-bit DACs and amplifiers.

→ Note that reference levels and offset errors must correspond to N·K bits resolution in order to achieve N·K bits.

Due to the S/H's, a new conversion can start as soon as the MSBs are converted. The output bits are then stored in shift registers

The first pipeline stage has the highest accuracy requirements.
To prevent the residue from the previous stage to over- or underflow the input range of the next stage, extended input ranges are used (redundant bits)

Example 1,5-bit subsystem implementation



Phase 1 V_k is sampled over C_F and C_S, V_{k+1} is latched

Phase 2
$$V_{k+1} = \begin{cases} \left(1+\frac{C_S}{C_F}\right)V_k - V_r\frac{C_S}{C_F}, & V_k > \frac{V_r}{4} \\ \left(1+\frac{C_S}{C_F}\right)V_k, & -\frac{V_r}{4} < V_k \le \frac{V_r}{4} \\ \left(1+\frac{C_S}{C_F}\right) + V_r\frac{C_S}{C_F}, & V_k \le -\frac{V_r}{4} \end{cases}$$