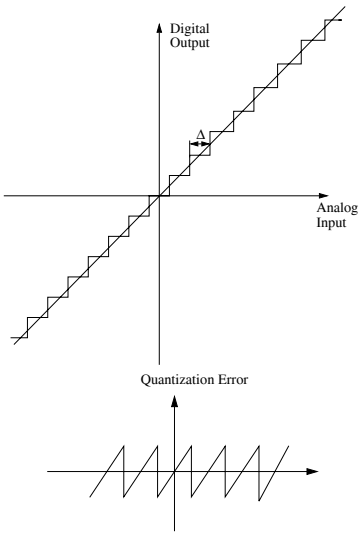
LECTURE 10

Quantization



If the quantization error is treated as white noise having equal probability of laying anywhere in the range $\pm\Delta/2$, its mean square value is given by

$$e_{rms}^2 = \frac{\Delta^2}{12}$$

If we have an N-bit converter the maximum amplitude of a sinusoidal input signal is $2^{N-1}\cdot\Delta$. The signal rms power is then given by

$$\frac{(2^{N-1}\cdot\Delta)^2}{2}$$

and the Signal-to-Noise Ratio (SNR) of an ideal ADC can be calculated as [59]

$$SNR = 2^{2N}\cdot 1.5$$

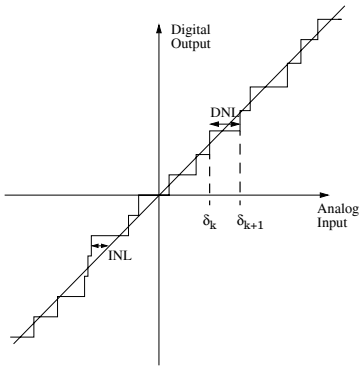
or expressed in decibels

$$SNR = 6.02\cdot N + 1.76\,\text{dB}$$

The SNR is thus increased by 6 dB per additional bit in the converter.

Nonlinearity

Due to non-ideal circuit elements in the actual implementation of the Converter the code transition points in the transfer function will be moved as illustrated below.



The step size in the non-ideal ADC deviates from the ideal size Δ and this error is called the Differential NonLinearity (DNL) error. This can be expressed as

$$DNL_k = \delta_{k+1} - \delta_k - LSB$$

where δ_{k+1} and δ_k are the actual transition points for code $k+1$ and k respectively and LSB is the ideal step size.

The total deviation of a code transition point from the ideal transition point is called Integral NonLinearity (INL) and can be expressed as

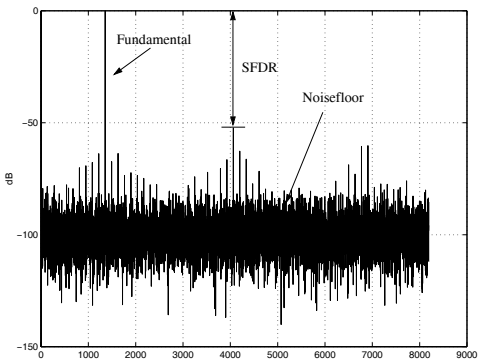
$$INL_k = \sum_{i=1}^{k} DNL_i$$

In some applications offsets and linear gain errors are acceptable and it is then common to specify the INL with respect to a best fit line rather than to the ideal transfer function. By doing so offsets and linear gain errors will not appear in the INL.

Some of the errors in the ADC is frequency dependent and thus the nonlinearity errors will be frequency dependent. The nonlinearity errors are usually measured using a low frequency input signal but can in principle be measured at any input frequency.

• Dynamic Specifications

For converters used in telecommunication applications the INL and DNL is not sufficient to characterize the performance. It is more convenient to characterize the performance in the frequency domain using measures as SNR and SFDR (see below). The dynamic performance is usually determined by using a single-tone sinusoidal input signal but sometimes multi-tone measurements are more informative. In the figure below is shown a typical FFT-spectrum of a 10 bit non-ideal ADC when the input signal is a single-tone sinusoidal.



The input signal appears as the fundamental in the FFT-spectrum and the quantization error generates a white noisefloor. The nonlineraities in the ADC cause harmonic distortion tones to appear above the noise floor where some of the harmonics are folded from higher frequencies due to the sampling process. Based on the FFT a number of measures to characterize

dynamic performance of converters can be defined.

Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range (SFDR) is the ratio of the power of the signal and the power of the largest spurious (distortion tone). SFDR is usually expressed in dBc, i.e.

$$SFDR = 10\cdot\log\left(\frac{\text{Power of the signal}}{\text{Power of the largest spurious}}\right)$$

Total Harmonic Distortion (THD)

The Total harmonic distortion is the ratio of the power of the fundamental and the total harmonic distortion power and can be expressed in dBc as

$$THD = 10\cdot\log\left(\frac{\text{Power of the signal}}{\text{Total Harminic Distortion Power}}\right)$$

Since there is an infinite number of harmonics the THD is usually calculated using the first harmonics or until the harmonics can not be distinguished from the noise floor.

Signal-to-Noise Ratio (SNR)

The Signal-to-Noise Ratio (SNR) is the ratio of the power of the fundamental and the total noise power excluding the first harmonic components and can be expressed in dBc as

$$SNR = 10\cdot\log\left(\frac{\text{Power of the signal}}{\text{Total Noisefloor Power}}\right)$$

Signal-to-Noise and Distortion Ratio (SNDR)

The Signal-to-Noise and Distortion Ratio (SNDR) is the ratio of the power of the fundamental and the total noise power and can be expressed in dBc as

$$SNDR = 10\cdot\log\left(\frac{\text{Power of the signal}}{\text{Total Noise Power}}\right)$$

Effective Number Of Bits (ENOB)

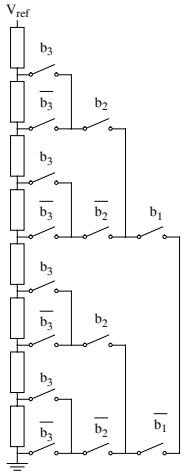
The Effective Number of bits (ENOB) is a measure based on the SNDR of an ideal ADC according to Eq. . The ENOB is determined by

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

where SNDR correspond to the actual (non-ideal) value.

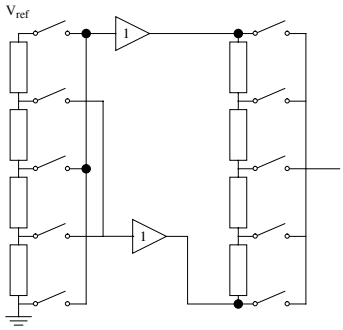
D/A Converters

• Resistor String Converters



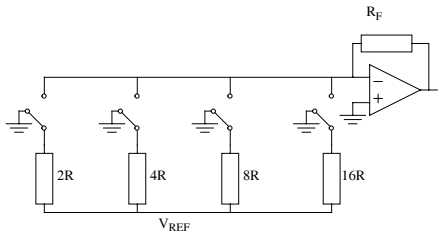
- The speed will be limited by the RC time constant for the switches. By using digital coding for the switch control signals the switch depth can be reduced to only one switch and the speed is thus increased.
- The number of components increases exponentially with the number of bits.

• Multiple R-String Converters



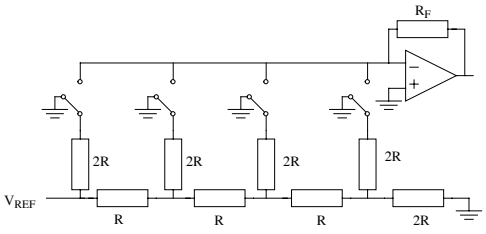
- The number of resistors is reduced.
- The accuracy requirements in the second string is smaller.

Binary Scaled Converters



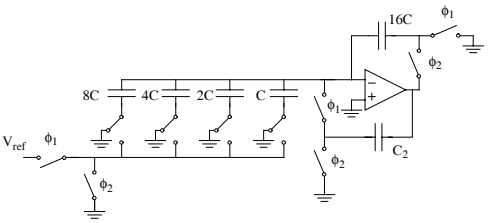
- Requires few switches and resistors
- Large difference between smallest and largest resistor size

• R-2R-Based Converters

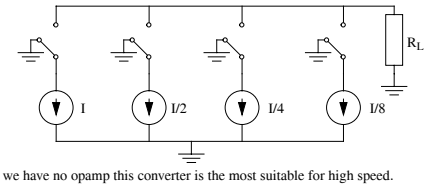


- Reduced Resistance ratio

• Charge-Redistribution SC Converter



• Current-Mode Converter



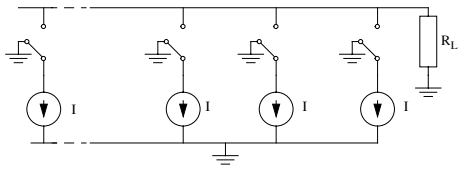
- Since we have no opamp this converter is the most suitable for high speed.

• Glitches

Due to different delays in the switch signals there may be glitches in the output signal which will reduce the SNR of the converter.

• Thermometer Code Converters

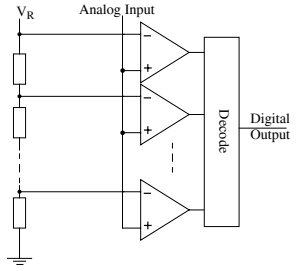
To avoid large glitches in the output signal the most significant bits can be implemented by using a thermometer code.



- The number of switches and current sources is 2^N
- A digital binary-to-thermometer code converter is needed

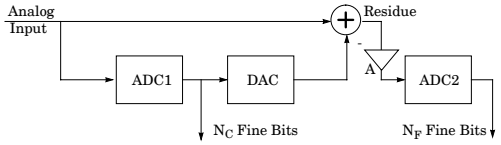
A/D Converters

• Flash Converter



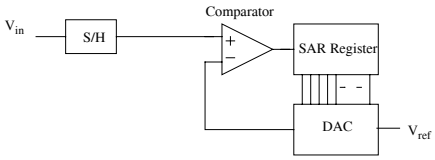
- High Sampling Rate
- The Number of Comparators is $2^N - 1$ => <10 bits

• Semi-Flash



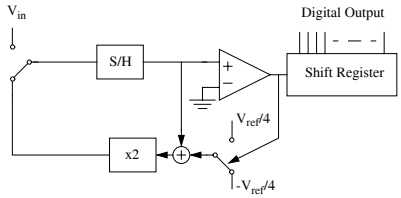
- Requires only $2^{N_C} + 2^{N_F} - 2$ comparators
- A DAC with $N_C + N_F$ bits accuracy is needed
- By using digital correction errors in the first ADC can be corrected

• Successive Approximation



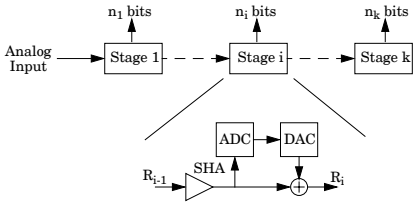
- Low speed converter. The speed is proportional to the number of bits.
- Only one comparator

• Algorithmic (Cyclic)



- Same speed as the successive approximation converter

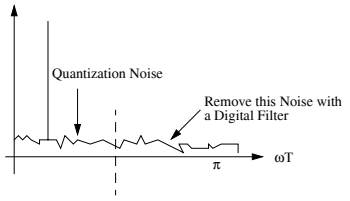
• Pipelined Converters



- High speed
- Less comparators than flash and semi-flash converters
- Digital correction to correct errors in the ADCs
- The required resolution is reduced in every stage

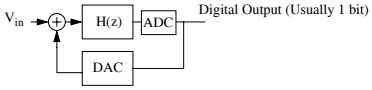
• Oversampling Converters

By using oversampling parts of the quantization noise can be removed with digital filters.



For every doubling of the oversampling ratio $OSR = \frac{f_s/2}{f_{in,\,max}}$ the SNR is improved by 3dB = 0.5 bits.

In sigma-delta converters noise-shaping is utilized to increase the resolution.

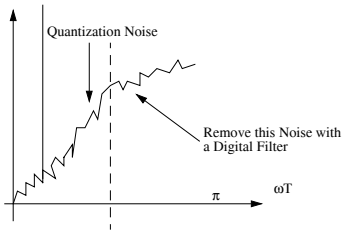


The transfer function for the input signal and the quantization noise is

$$H_{in}(z) = \frac{H(z)}{1 + H(z)} \text{ and } H_{noise}(z) = \frac{1}{1 + H(z)}$$

By choosing $H(z) = \frac{1}{z-1}$ (an integrator) the signal transfer function is a all-pass function and

the noise transfer function is a high-pass function.



By increasing the order of the filter more bits are gained. For every doubling of the OSR we gain L+0.5 extra bits of resolution, where L is the order of the filter.