LINKÖPING UNIVERSITY
Department of Electrical Engineering

TSIU03, SYSTEM DESIGN

LECTURE 9

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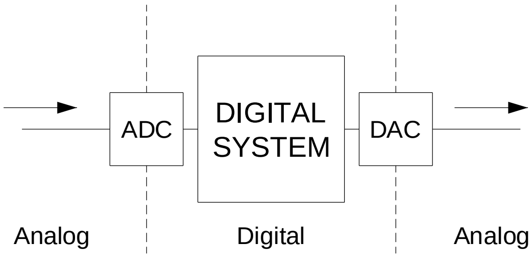
TODAY

- Signal Processing.
- Variables.

ADC, DAC

- ADC (Analog-to-digital converter): device that converts an analog (physical) signal (usually voltage) to digital values.
- DAC (Digital-to-analog converter): device that convert digital values to an analog signal.



SAMPLING

- Sampling: reduction of a continuous (analog) signal to a discrete one.
- Samples: The digital values that represent the values of the analog signal.
- Sampling frequency (f_s): number of samples per second taken for a continuous signal to make a discrete signal.
- Sampling period (T_s): Time between two consecutive samples.

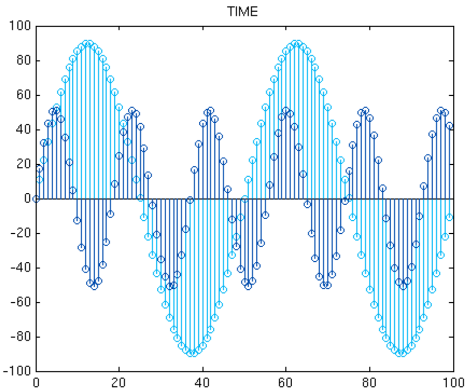
$$f_S = \frac{1}{T_S}$$

- **Nyquist Theorem**: The sampling frequency must be at least twice the maximum frequency of a signal, in order to be able to reconstruct that signal:

$$f_S \geq 2 \cdot f_{MAX}$$

EXAMPLE

- Here we can see two signals in the time domain with different frequencies and different amplitudes. Which is the amplitude and the frequency of each of the signals?
- If both signals happen at the same time, the sample at that time will be equal to the sum of their values at that time.
- The binary number in our system at a certain clock cycle is just the value of the sample at that time.



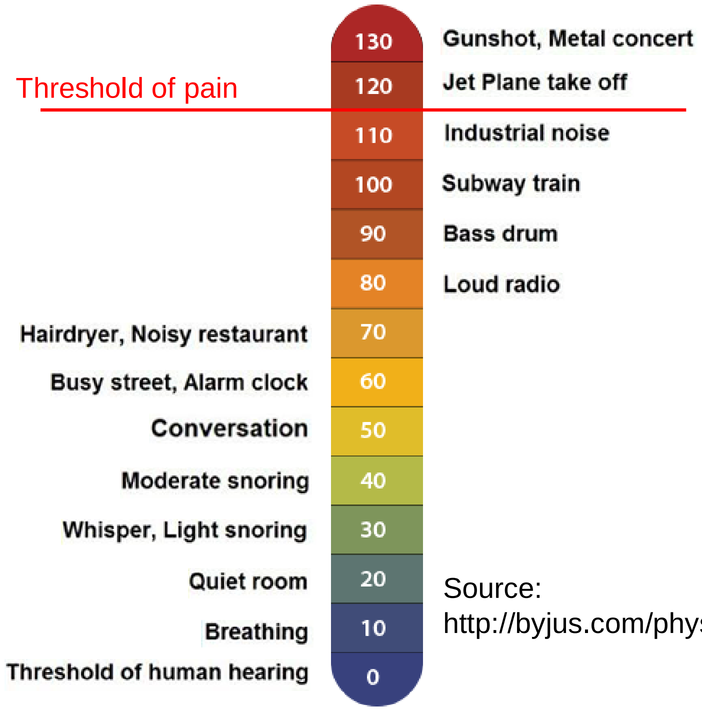
DECIBELS

- Decibels are a logaritmic unit used to express the ratio of two values of a physical quantity. Sometimes one of the values is a reference value, such as for sounds.
- As it is a ratio between two values of the same physical quantity, decibels do not have any physical dimension.
- When the ratio is large, it allows for working with small numbers instead of large values.
- We generally use decibels to relate the power of two signals.
- A multiplication in linear units corresponds to an addition in decibels.

$$\Delta P(dB) = P_O - P_I(dB) = 10 \cdot \log_{10}\left(\frac{P_O}{P_I}\right) = 10 \cdot \log_{10}\left(\frac{V_O}{V_I}\right)^2 = 20 \cdot \log_{10}\left(\frac{V_O}{V_I}\right)$$

$$\frac{V_O}{V_I} = 10^{\left(\frac{\Delta P(dB)}{20}\right)}$$

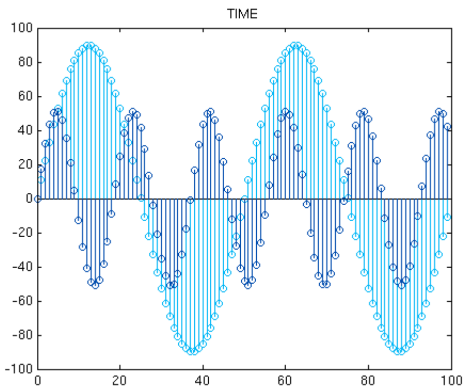
DECIBEL SCALE

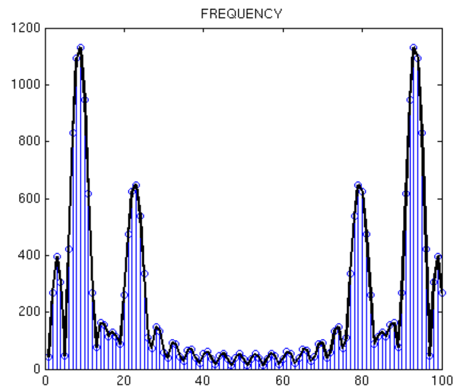


Source:
http://byjus.com/physics/decibel/

TIME vs FREQUENCY

- In the frequency domain (to the right) we see the spectrum of both signals together happening together. This may be two musical notes played at the same time.
- How can you see the frequency and the amplitude in the frequency domain?





MULTIPLYING WITH FRACTIONS

- Multiplications with fraction when having unsigned and/or signed values
  - Values often interpreted as integers
- Multiplication with fractional values
  - Rewrite coefficient to be a large integer 2^k and then multiply with $1/2^k$
- Example: multiply and 8 bit signed value with constant 0.75
  - 0.75 = 0.75*4/4=3/4
  - Multiply first input with 3 (=> 10 bit signed value)
  - Divide result by 4 => shift result two steps to the right. Result now 8 bit

VARIABLES

- Variables can only be used inside a process.
- They can have any data type (as is true for signals and constants).

```
process (clk, rst)
  variable m: integer;  -- declaration similar to signals
  begin
  if rst = '1' then
     m := 0;             -- Initialization using :=
  elsif rising_edge (clk) then
     m := a;             -- To assign values, we use :=
   ...
```

- **IMP:** signals are not updated during process execution (only at the end of the process), but variables are updated during process execution, i.e., they can store temporary values.
- Limited use in VHDL: If you want to create a connection in the circuit, use a **signal.**

SIGNALS v.s. VARIABLES

- What do these two pieces of code do when they are included in a process with clk in the sensitivity list?

```
if rising_edge (clk) then
  q <= q + 1;
  if enable = '0' then
    q <= q;
  end if;
end if;
```

```
if rising_edge (clk) then
  q := q + 1;
  if enable = '0' then
    q := q;
  end if;
end if;
```


RESOURCES FOR THE PROJECT

- Project folder:

  - There is a private folder for each group. It is already created and every member of the group has access to it.

  - Please, keep the files of the group in the folder (VHDL files as well as the project documents).

  K:TSIU03\Groups\Group_XX

- Free Altera tools available online:

https://www.intel.com/content/www/us/en/programmable/downloads/download-center.html

  Select version 13.0 service pack 1

- Free tools to simulate simple circuits: Atanua, CEDAR Logic.
- Free tool to draw circuits: Dia Diagram Editor.

CHECKLIST FOR LECTURE 9

- ADC, DAC, sampling, time and frequency, decibels.
- VHDL: variable, :=

AT HOME

- Review the checklist for lecture 9 and check that you understand all the concepts and you know how to use them.
- Go through the checklists of all the lectures to check that you understand all the concepts in the course.

NEXT LECTURE

- Guest lecture given by Jose Nunez-Yanez
- Summary of VHDL