

VLSI Chip Design Project TSEK06

Project description and requirement specification

Version 1.0

**Project: An 8-Bit Successive Approximation
Analog-to-Digital Converter**

Project number: 6

Project Group:

| Name | Project members | Telephone | E-mail |
|------|----------------------------------|-----------|--------|
| | Project leader and designer 1(5) | | |
| | Designer 2(5) | | |
| | Designer 3(5) | | |
| | Designer 4(5) | | |
| | Designer 5(5) | | |

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1 Background

Low-power ADCs are highly demanded in battery-powered or portable communication devices. Successive-approximation (SA) analog-to-digital converters (ADCs) are power-efficient due to its simple architecture with only one comparator in the whole system. This document describes the design specification of a low-power 8-bit SA ADC at a sampling rate of 1-MS/s.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. In the project, students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

| | |
|--|---------------|
| 1: Project selection | Week 3 |
| 2: Pre-study, project planning, and discussion with supervisor | Week 4 |
| 3: High-level modeling design and simulation result (report) | February 11 |
| 4: Gate/transistor level design and simulations result (report) | March 11 |
| 5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations. | May 6 |
| 6: DEADLINE , Delivery of the completed chip. | May 13 |
| 7: DEADLINE , Final report, and oral presentation | May 24 |

1.3 Parties

The following parties are involved in this project:

- 1- Customer: Dai Zhang
- 2- Project supervisor: Dai Zhang

Tasks:

- Formulates the project requirements.
 - Provides technical support.
 - Reviews the project documents.
- 3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way.
- Organizes the team meetings as well as the meetings between the team and supervisor.

- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**).
- 4- Project design members (including the project leader)
- Are equally responsible for project planning and design.
 - Participate actively in all the meetings.
 - Support the team and the project leader.
 - Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 Basic understanding of SA ADC

A single-ended SA ADC, shown in Figure 1, consists of a sample-and-hold (S/H) circuit, a digital-to-analog converter (DAC), a comparator, and a successive approximation register (SAR). It is designed based on the binary-search algorithm.

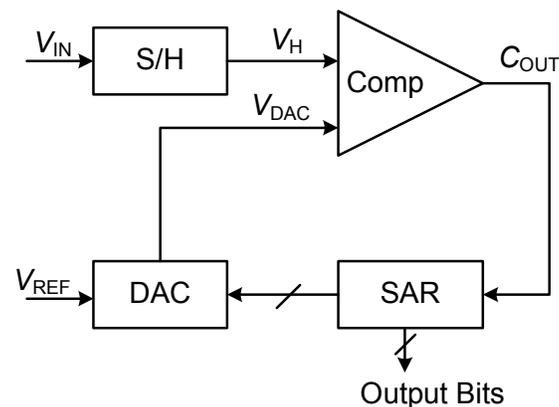


Figure 1: Block diagram of SA ADC

Figure 2 shows an example of the timing diagram for an 8-bit SA ADC. At the first clock cycle, the input voltage is sampled by the S/H circuit, and both the SAR and the DAC are in reset phase. The conversion starts from the most-significant-bit (MSB) at the second clock cycle. The SAR makes a guess '1' for the MSB and sends the digital information to the DAC. The DAC outputs a voltage of $V_{REF}/2$ accordingly. Then the comparator does the comparison between the hold voltage V_H and the DAC output V_{DAC} . At the next conversion cycle for MSB-1, the SAR loads and stores the previous decision for MSB and again makes a guess '1' for MSB-1. The digital word sent to the DAC contains both the previous decision and the current guess. As the clock cycles increase, the output of the DAC successively approximates the sampled voltage. One bit is obtained per clock cycle.

The SAR control logic is a sequential finite state machine, which generates the approximation sequence of 9 steps, given by Table 1. As explained above, step 0 is the sampling step. For the generic step ($s = 1 \dots 8$), three operations are performed: 1) it makes a guess '1'; 2) it loads the decision bit from the comparator; 3) it stores the determined bit which generated at $s-1$ step.

Successive Approximation ADC

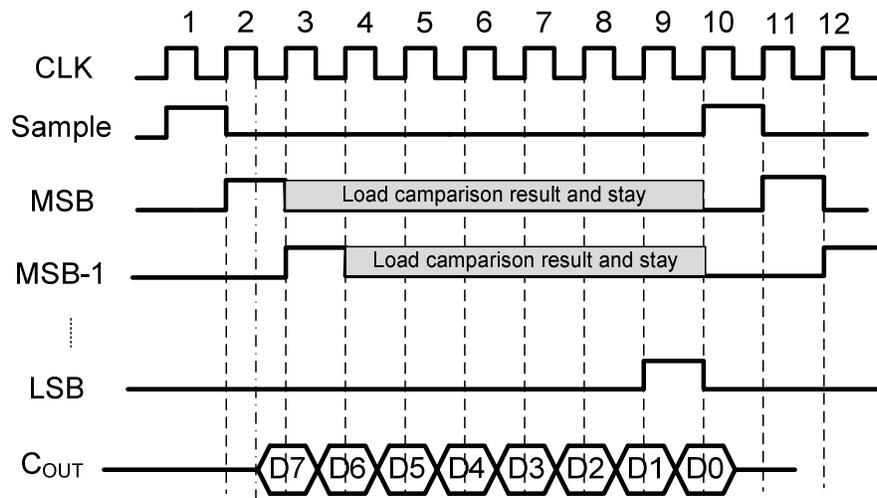


Figure 2: Timing diagram of 8-bit SA ADC

Table 1: SAR algorithm for 8-bit ADC

| Step | SAR | | | | | | | | Sample | C _{OUT} |
|------|-----|----|----|----|----|----|----|---|--------|------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D7 |
| 2 | D7 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D6 |
| 3 | D7 | D6 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | D5 |
| 4 | D7 | D6 | D5 | 1 | 0 | 0 | 0 | 0 | 0 | D4 |
| 5 | D7 | D6 | D5 | D4 | 1 | 0 | 0 | 0 | 0 | D3 |
| 6 | D7 | D6 | D5 | D4 | D3 | 1 | 0 | 0 | 0 | D2 |
| 7 | D7 | D6 | D5 | D4 | D3 | D2 | 1 | 0 | 0 | D1 |
| 8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | 1 | 0 | D0 |

2.2 System description

In this project, a differential SA ADC, shown in Figure 3, will be implemented in order to have good common-mode noise rejection. Moreover, the capacitive DAC also realizes the sample-and-hold function to save power.

The DAC is implemented with a binary-weighted capacitive array and it follows the charge-redistribution principle during conversion. The comparator is implemented with a dynamic latch circuit in order to avoid static bias current, thereby further reducing the power consumption.

Successive Approximation ADC

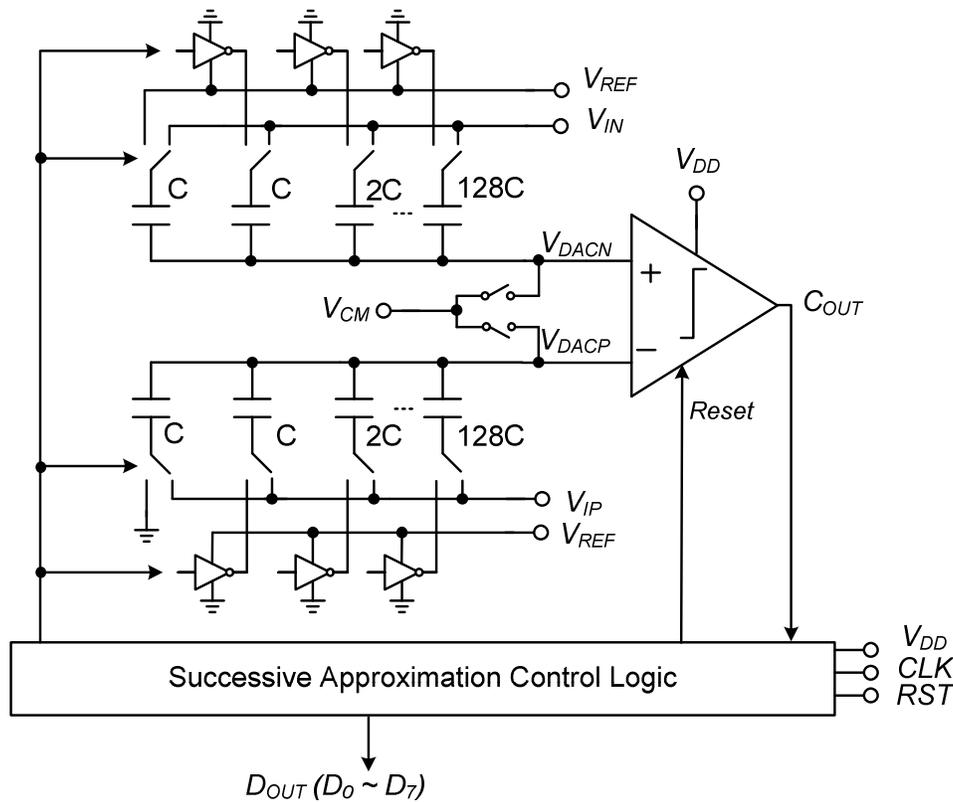


Figure 3: Block diagram of an 8-bit differential SA ADC

2.3 Important design metrics

The ADC should be designed for a sampling frequency of at least 1 MHz and it is aimed for low-power application. Moreover, the performances of the ADC need to be evaluated.

Important things to be considered are:

- Errors caused by sampling
- Matching of the capacitive DAC
- Speed and resolution of the comparator
- Total time budget of the ADC
- Power consumption of the ADC
- Testing of the ADC

3 Area and performance requirements

Table 2 summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Table 2: Circuit performance requirements

| Requirement | Requirement text | Priority |
|-------------|--|----------|
| 1 | Sampling frequency at least 1 MHz | High |
| 2 | Evaluate the performance of ADC | High |
| 3 | Low power optimization | Medium |
| 4 | Layout matching | High |
| 5 | Integrate as many system components as possible on-chip | High |
| 6 | Schematic and layout must be verified by simulation | High |
| 7 | Chip core area $< 0.27\text{mm}^2$ (shown in Figure 4) | High |
| 8 | Total project pin count ≤ 11 | High |
| 9 | Design technology is AMS 4-Metal $0.35\mu\text{m}$ CMOS | High |
| 10 | The most important system nodes should have off-chip access pins | Low |
| 11 | On-chip current densities $< 1 \text{ mA}/\mu\text{m}$ | High |
| 12 | All requirements fulfilled in “ <i>typical</i> ”, “ <i>slow</i> ”, and “ <i>fast</i> ” process corners and for temperatures between 25°C and 110°C | Medium |

3.1 Available resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, <http://www.bibl.liu.se/english/databas/>

3.2 Tools

- Circuit simulation and layout tools from Cadence[®], <http://www.cadence.com/>
- Digital signal processing tools from Matlab[®], <http://www.mathworks.com/>

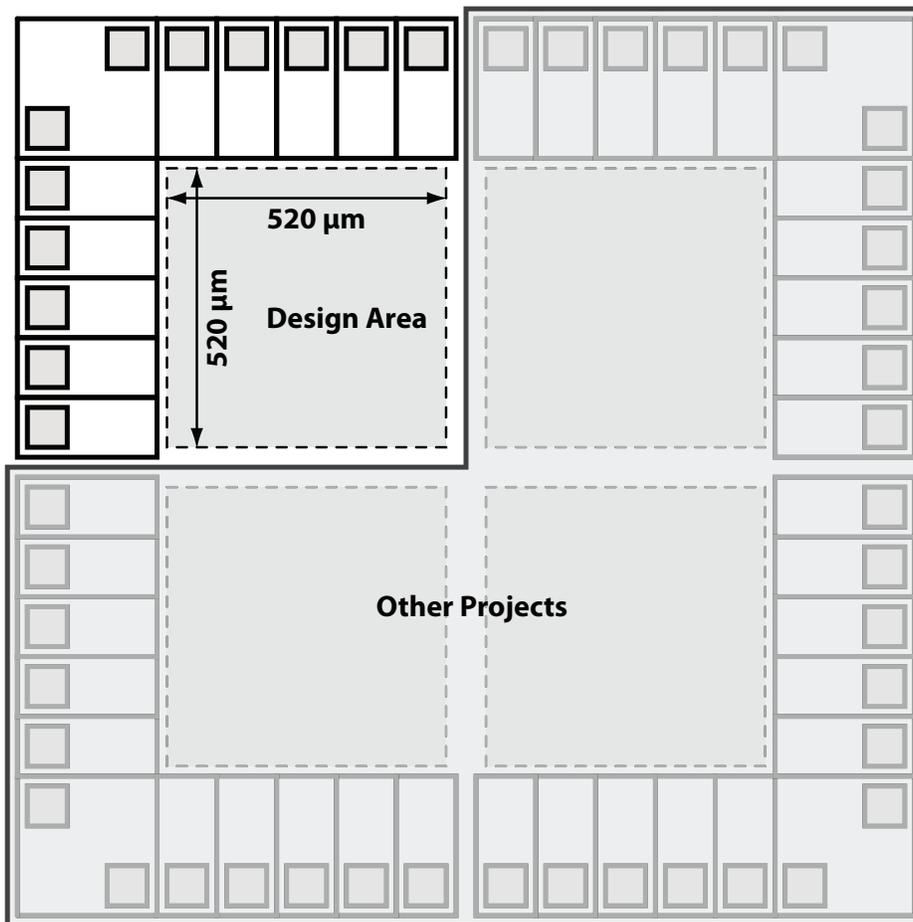


Figure 4: Schematic picture of a 3mm² chip highlighting one corner with 10 generic pads, one V_{DD} and one V_{SS} pad (total 12 per group). Four groups will then share one chip.

4 References

- Maxim, “Understanding SAR ADCs”, Application Note 1080, Mar 01, 2001.
- K. H. Lundberg, “Analog-to-Digital Converter Testing,” <http://www.mit.edu/people/klund/A2Dtesting.pdf>, accessed: Jan. 2013.
- J.M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 1st edition, 1999.

For more literature references consult with your supervisor.