# Project Guide

## TSEK06 VLSI Chip Design Project and TSEK11 Evaluation of an IC

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# 1 Introduction

This document provides a guide for how to complete the project part of the course VLSI Design Project (TSEK06) and Evaluation of an Integrated Circuit (TSEK11). The guide contains recommendations and requirements that should be fulfilled in order to complete the project. Moreover, the guide aims to organize and give structure to the flow of the project for the participating students and eases the documentation part.

## *1.1 Project Purpose*

This course aims to give a comprehensive introduction to:

- Design and fabrication of full-custom, high-performance, low-power VLSI circuits in sub-micron CMOS technology.
- VLSI design methodology.
- Advanced circuit techniques, chip layout and chip design.
- Various commercial CAD tools being used in industry.

Further, the course promotes teamwork and communication skills required to run large and complex VLSI projects. Therefore, we support the CDIO project and the LIPS model [1] for project planning documentation.

# 2 Project Members

In an industrial project there are several participating persons with different roles in the project.

The structure of the project in this course is similar to the one used in chip design outside the university. We have a customer or sponsor that orders and pays for the project. There are project group members, including a project leader, that are responsible for completing the project. In an industrial project there are also experts that can be consulted regarding various issues.

## *2.1 Sponsor*

The role of the sponsor is to order a project and provide the financial resources to the project group. A sponsor tells us what he/she wants. This is often a high-level description such as: "I want an analog-to-digital converter with the following data…" or "I would like to have a special-purpose microprocessor very good at doing…"

It is always up to the sponsor to determine if the completed project or project parts are carried out according to the specifications. It is therefore important that the sponsor is kept updated about progress of the project and is informed about possible changes in the specification. The sponsor is always eager to know the time plan of the project and wants to know of risks that may result in delays and project failure. The sponsor can be an external customer arriving at our company knowing nothing about VLSI or a member of the company, usually connected to the marketing department.

In this course the project supervisor will act as the sponsor. Even though this is not always the case, in this course the project specification will be provided by the sponsor.

## *2.2 Project Leader*

The role of project leader is to plan the work and to create a working environment where the members of the project work efficiently towards the same goal. The project leader is also responsible for keeping the sponsor updated, making sure that documentations are up to date, and for planning and setting up meetings. Together with the group members the project leader is responsible of the completion of the project. The goal of the project is that all members of the group should learn the art of IC design, which means that the project leader should participate in the design work on the same terms as the rest of the group members.

## *2.3 Group Member*

The group members can, apart from being co-responsible of the design work, be appointed different roles. These roles can for instance be: document responsible, chip integration responsible, tape-out responsible, presentation responsible, and verification responsible.

## 2.4 Consultant

Usually, the project group cannot be expected to know everything related to the project. It is quite common to use external consultants and experts that assist the project group. In this course the supervisor will apart from the sponsor role also act as a consultant.

# 3 Project Phases

A large-scale VLSI design project can be divided into the following steps, shown in Figure 3-1.

## 3.1 Step 1: Literature Search

We have to avoid spending valuable time in reinventing the wheel over and over again. If we have been running a project earlier, very similar to the system that our sponsor asks for, of course we will use our experience in this field. If we do not have this experience, we can borrow it from other people by reading their reports (including library search). Another opportunity is the market of "Intellectual Properties" (IP's), where one can purchase a well-documented and verified IP core (see http://www.design-reuse.com). Such an IP core might be embedded in our design to reduce the design cycle. However, this is not a case in this course.

Questions to answer in this stage of a project are:

- What has been done before?
- How was it done?
- Do patents control earlier inventions?
- Are there any relevant IP's offered on the market?

## 3.2 Step 2: Brain-Storming and High-Level System Description

In the literature search, we will probably not find exactly what we want and then we have to think. The first thing to do is to develop a high-level description of a system, which has the same behavior as the system that the sponsor asked for [2], [3]. For this purpose, you can use behavioral simulators where models are described in VHDL-/AMS or Verilog-/A, which are so called hardware description languages. To some extent, MATLAB with its utilities is an alternative tool. If behavioral descriptions can be made, this system should be simulated in order to verify that it behaves as we intended when we developed it. When we have built and successfully simulated the system, it is of great help to show the system behavior to our sponsor. We must be sure that this is the intended behavior before we continue with the project. At this level, it is impossible to guarantee e.g. timing constraints, which therefore have to be estimated.

## 3.3 Step 3: Top-Down Methodology and Further Brain-Storming

The high-level description from step 2 is developed and refined to include more details [2]. When more details have been included, we need to simulate again and verify that the behavior is still the same as for the model approved by the sponsor. This is an iterative process going from block-level description via gate or macro-model level to transistor-level implementation of the circuit. Of course, intermediate levels, where some parts of the design are described with blocks and other parts are described with transistors, are common. The main workload here is simulation, simulation, simulation and some circuit development. If we discover that the circuit does not fulfill the requirements according to the specifications, we need to return to a description on a higher level, change the design at this level appropriately and then develop new low-level models. Meanwhile, we simulate again and again to make sure that the behavior of the top-level system is maintained.

Also, at this step you have to make your design testable. This means that it should be possible to access selected internal nodes of your IC after manufacturing. Previous years, some groups have detected errors during measurement of the fabricated chips. Possible malfunction of a chip or its low performance might be due to unexpected fabrication defects, too large process tolerances, or due to careless design verification that might be your fault. Apparently, in such a case the chip needs a diagnosis procedure to identify the existing failures. In a design practice, one adds an extra circuitry to a chip to facilitate test, i.e. to provide so-called controllability and observability to a circuit via selected nodes. Different techniques, such as boundary scan test, are referred to as design-for-testability (DfT) (IEEE Std. 1194.1 for digital and 1194.4 for analog and mixed-signal ICs). For more details you can refer to [3].

Your design must be testable!

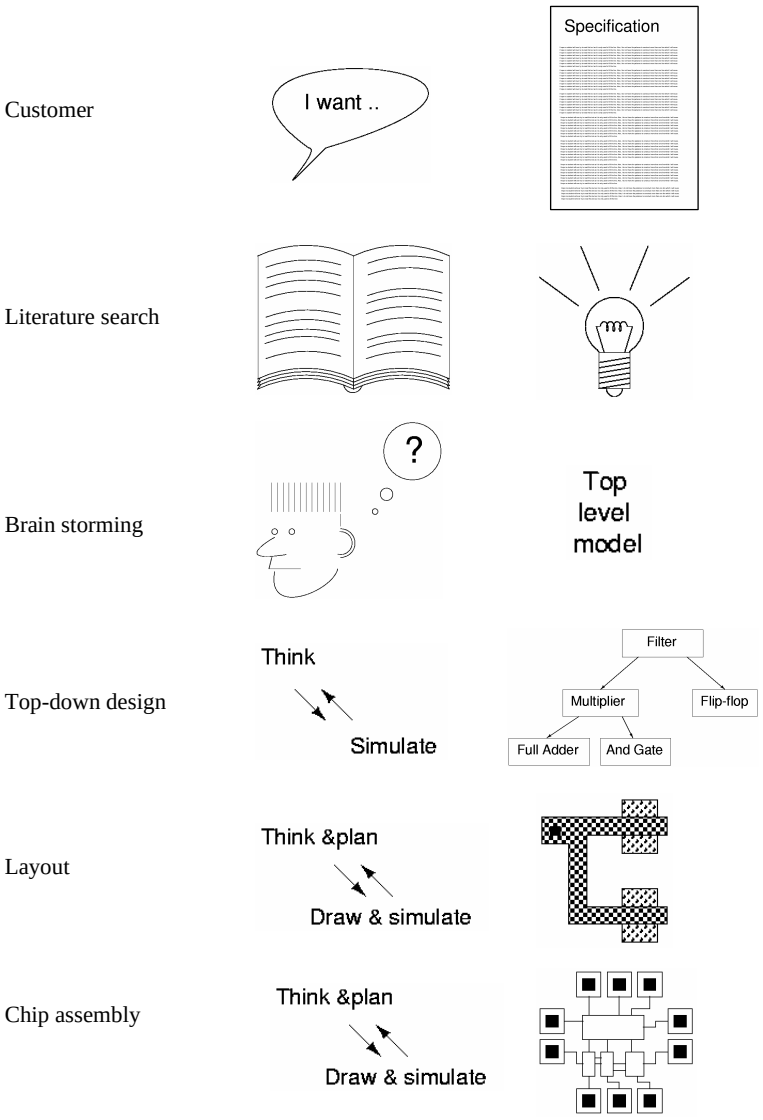



**Figure 3-1: VLSI design project flow.**

## 3.4 Step 4: Layout

This part of the project is the reverse of step 3 and some people call it bottom-up design. Here we start to build small cells with transistors, contacts, and wires as the smallest building objects. When some small cells have been built, larger cells are composed with these sub-cells as building blocks. This gives a hierarchical design structure, which greatly speeds up the chip design. Once we have built a D-flip-flop or a logical gate, we use them in many other blocks and, hence, avoid building many gates with the same functionality. Of course we cannot manage to do this without simulations. When the layout of a D-flip-flop is finished, we do a layout extraction and run it through the simulator to verify that the D-flip-flop is working correctly. If not, we have to find the error(s) and correct the layout.

## 3.5 Step 5: Chip Assembly

Unfortunately, some people (students) think that the project is finished when the layout of the top cell is done. After this step we still have 10-20 % left of our project! When the top-level block has been built and verified by simulations in step 4, we need to add some circuits so that the block can communicate with the off-chip hardware. There are a few things to consider here.

A bonding wire (electrical connection from the surrounding world) has a diameter of about 25-50 µm and the accuracy when connecting the wire to the chip surface might be ±20 µm. Contacts and wires used in the circuit design have dimensions of about 1 µm. Therefore, we place large (100x100 $\mu m^2$) pieces of metal (PADs) to which the bonding wires are connected [2], [3].

Internal capacitive loads inside a circuit are about 10-50 fF, which often can be driven by a minimum-sized transistor. Even though the on-resistance of a transistor is 1-3 kΩ, the delay will be in the order of 1 ns. The capacitive load when transferring a signal off-chip to the surrounding world is about 10-50 pF, which indicates that we need a transistor 1000 times stronger to drive the off-chip load. Therefore, output buffers are necessary when the circuit is sending information out from the chip.

The capacitive load of an internal signal inside a circuit is proportional to the number of transistors it is connected to. The clock signal often has a large fan-out and consequently a large capacitive load. If a large capacitance is driven by a bonding wire, we end up with a LC circuit (bonding wire = inductance, internal load = capacitance) working as a low-pass filter. This low-pass filter tends to smooth out sharp edges of the signal, which might cause logical errors inside the circuit. Therefore, it is necessary to restore the edges of the signal by internal clock drivers.

Electrostatic discharge (ESD) might be very harmful to CMOS circuits since it can introduce permanent errors. The reason for this is that the gate of a MOS transistor is electrically disconnected from the source and drain by a very thin layer of gate-oxide (5-15 nm), which has a breakdown voltage of about 4-15 V. Charge stored on fingertips can introduce voltages in the order of hundreds of volts. To avoid oxide breakdown in chips, the input and output pads are often provided with protection circuitry.

When all these features have been added to the circuit, we have a final chip layout that should be simulated once again to verify correct functionality.

## 3.6 Step 6: File Preparation

The file format we are working with when designing a chip includes information about transistors, wires, signal names, and other textual information. The chip-manufacturing company only needs information about different layers. Therefore, we have to convert our layout files into a “layer file” in a binary format. When doing this, some errors might be discovered and we have to correct our layout file.

## 3.7 Step 7: Testing of Chips

The chip design is not finished until we have proven that the chip is working! Since it takes a few months to manufacture the chips, we cannot include the chip testing in the course TSEK06 VLSI Design Project. Instead, there is a separate course TSEK11 Evaluation of an Integrated Circuit in the fall in which you can test the chips designed in this course.

# 4 Documentation

In the course TSEK06 there is a requirement of three report documents. These reports should be considered as a status report to a sponsor with technical knowledge (i.e. the supervisor). The purpose of the report is to keep the sponsor informed about the project progress, that the specification will be fulfilled, any risks that might jeopardize the project and the costs of the project (i.e. time spent). A fourth report will be required in order to pass the follow-up course TSEK11 Evaluation of an IC.

## 4.1 High-Level Design Report

This is the first of three documents in the course TSEK06. This report should be handed in to the sponsor (i.e. supervisor) before the first tollgate meeting (Tollgate 1 / Milestone 1). The following part should be included in the report.

### 4.1.1 Time Plan

The time plan is where the group specifies how much of the resources that should be spent on each activity in the project. The group should have completed a preliminary time plan on their first meeting for the main parts of the design project. The time plan included in the high-level report should be updated and include time allocation for each part of the project. It should also be specified what each group member should do and how much time that he/she should spend on each activity. The time plan is of course a dynamic document that should constantly be updated. However, the group should strive to keep the original time plan as much as possible.

### 4.1.2 Time Report

In order for the sponsor (i.e. supervisor) to keep track of the project progress a time-report must be included in the high-level design report. The time-report should include how much time each group member spent on each task.

### 4.1.3 Block Level and Description

The high-level design report should include the complete block level description of the project. All blocks used must be motivated and described clearly. HDL code of specific blocks can be added if they add to the clarity, but as a general rule the amount of HDL code in this report should be minimized. Instead, describe the functionality of each block in words and/or with tables and expressions (i.e. Boolean expressions for combinatorial gates). Each sub-block should have its corresponding block specification, which will be used in the transistor design phase.

### 4.1.4 Simulation Results

High-level simulations verify that the topology and structure of the project is functional. At this stage of the project, it is important to design and implement the test-benches and test-cases for each block in the project. This will ease the simulation and verification work in the later sections in the design process. Moreover, the high-level simulations provide the means to determine block interface conditions.

In the report, simulation results that verify the desired functionality should be provided. Moreover, it is important to show simulation results that show that the blocks work together.

### 4.1.5 Risks and Delays

During the process of developing the high-level description of the project, potential problems and risks in the project might emerge. All such risks and potential problems should be well documented in the status report. Changes in specifications must be approved by the sponsor (i.e. supervisor) and the decision to approve or reject an altering of the specifications is usually based on the documented risk analysis.

## 4.2 Transistor Design Report

This is the second document in the course TSEK06. This report should be handed in to the sponsor (i.e. supervisor) before the second tollgate meeting (Tollgate 2 / Milestone 3). The following parts should be included in the report.

### 4.2.1 Time Plan

The instruction for the time plan is described in section 4.1.1.

### 4.2.2 Time Report

The instruction for the time report is described in section 4.1.2.

### 4.2.3 Block Level and Description

The transistor design report should include the complete block level description of the project. All blocks used should be motivated and described clearly. Transistor schematics of leaf-cells should be added in the report together with a discussion of transistor sizing strategies and choices. However, to limit the amount of schematics shown in the report, transistor schematics of standard gates (i.e. NAND, NOR, etc.) could be omitted and only described verbally. Each sub-block should also have its corresponding block specification.

### 4.2.4 Simulation Results

Transistor level simulations verify that the topology and structure of the project is functional and that the design works according to specification. The sub-blocks are simulated using the test-benches developed in the high-level design part. If sub-blocks need to be further divided, new test-benches should be implemented.

Simulation results that verify that the design works according to specification should be included in the report. Moreover, simulation results that show that the blocks work together is important to show.

### 4.2.5 PAD Assignments / Early Test Plan

Circuit nodes that will be measured should be identified early. The limited amount of contacts from the chip requires that the PAD assignment is thought through in detail. A test plan that specifies external voltages and currents, and how they behave, is also needed. Both PAD assignment and test plan need to be included in the transistor design report.

### 4.2.6 Risks and Delays

All the risks that where identified during block level design should be followed up. If the risks remain, they need to be documented in the transistor-level design report as well.

## 4.3 Final Project Report

This is the third and final document in the course TSEK06. This report should be handed in to the sponsor (i.e. supervisor) before the third tollgate meeting (Tollgate 3 / Milestone 6). The following parts should be included in the report.

### 4.3.1 Time Report

The final time report must include a list of how much time each group member has spent on each task.

### 4.3.2 Project Description

Here a short description of the project should be given with motivation and goals. Also include the block level descriptions from the previous reports (updated).

### 4.3.3 Simulation Results

The final project report should include all the essential simulation results. For instance the result of a typical test vector being applied to the complete chip. Simulation results from the test-bench of the entire chip including PAD-frame should be shown.

### 4.3.4 Evaluation Plan and PAD List

This part of the project report should include an extensive plan on how to evaluate the chip. The PAD frame should be accompanied with a PAD-list that explains the type of PADs used and the purpose of each pin. Moreover, a PCB sketch that explains how each pin should be connected to external parts should be included.

### 4.3.5 Risks

Even though the chip is successfully implemented there are still risks that might lead to chip malfunction. Potential risks should be documented.

### 4.3.6 Project Evaluation

The project evaluation should include a brief description of what the project group and its members have learned during the project. The group should also evaluate its own work, that is, how the project group has functioned, if the design work has been smooth, and how well the resources (time) have been spent. What were the good parts, what parts did not turn out so good? What would you change if you would do the project again? In this section of the report you can also include any course evaluation comments you have. How can we improve the course, what was good, what parts need improvements?

## 4.4 Chip Evaluation Report (for TSEK11)

For those students that choose to attend the follow-up course Evaluation of an Integrated Circuit (TSEK11) a fourth report is required. This report should be handed in to the sponsor (i.e. supervisor) before Tollgate 4 / Milestone 8. The following parts should be included in the report.

### 4.4.1 Project Description

Here a short description of the project should be given with motivation and goals.

### 4.4.2 Measurement Setup

Show the PAD list and PAD-placement. Discuss how the PCB has been soldered, which components have been used, and how they have been used. A list of instruments used and the test setup is also required.

### 4.4.3 Measurement Results and Comparison

Include the important measurement results and compare too the simulated data of your circuit.

### 4.4.4 Evaluation

The project evaluation should include a brief description of what the project group and its members have learned during the evaluation course. What can be improved in the design?

## 4.5 General Tips and Recommendations for Reports

Reports are much better if they include clear and illustrative pictures. Below are some tips of how you can include schematics, simulation results, and layout pictures in your reports.

### 4.5.1 How to Convert Schematics from Cadence to the Report

Just making a screenshot from Cadence of the transistor-schematic or block-schematic is usually not a good way to create nice pictures or figures. An example can be viewed in Figure 4-1. Here, a large schematic is taken directly from Cadence.

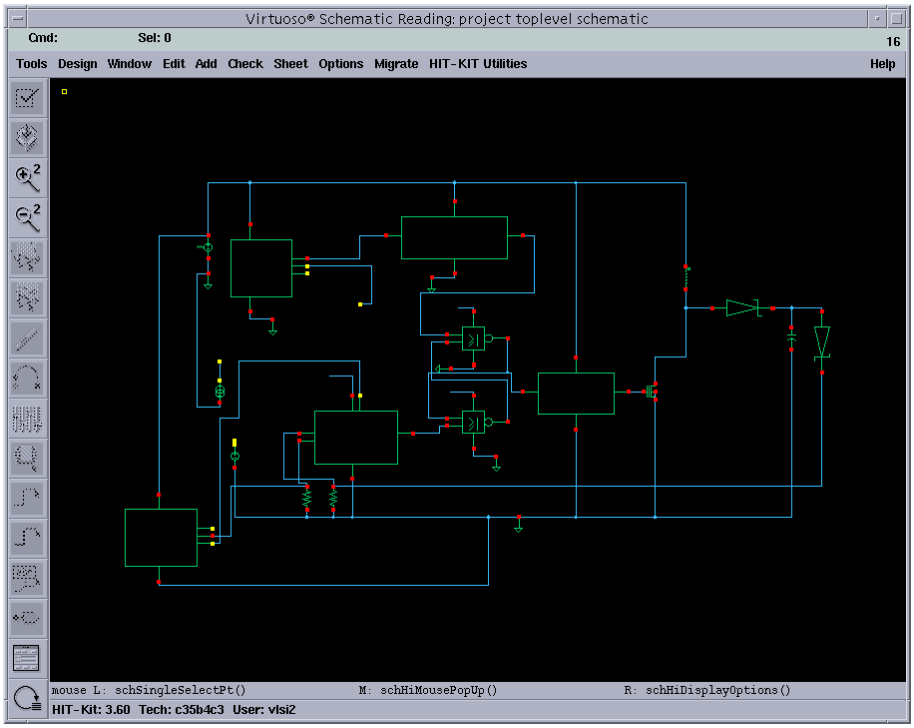



**Figure 4-1: Example of <u>not</u> so good schematic figure.**

Nonetheless, a snapshot is a good tool if it is used the right way. Smaller schematics are suitable to export to the word processor directly from Cadence. This can be done either with the snapshot function or by printing the schematic to a PostScript file that later can be transformed to any format recognized by the word processor. In Figure 4-2 a smaller schematic in gray scale is shown, which has been exported from Cadence with snapshot and then had its colors inverted.

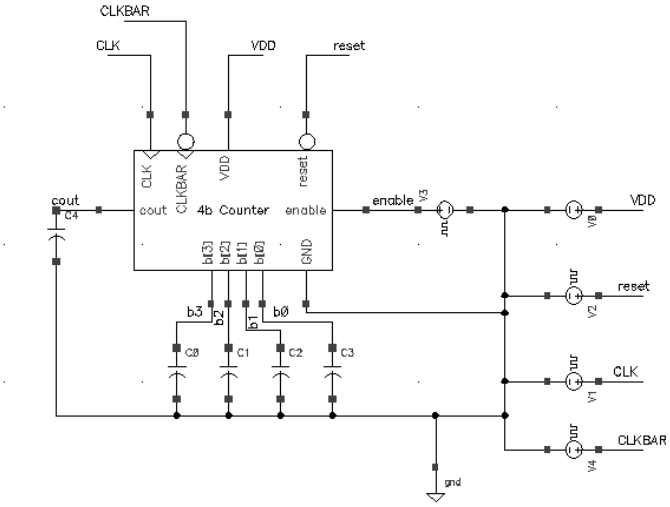



**Figure 4-2: A grey scale schematic taken with snapshot from Cadence.**

A second approach to get good pictures is to draw the schematic in some drawing software. A way that works very well together with *MS Word* is to use the draw function in Word. However, it takes some time to get used to the tool, but the result is often good. Insert a word-draw object by clicking *Insert -> Object… -> Word Picture*. An example of a schematic drawn with the draw function in MS Word is shown in Figure 4-3. The advantage with this kind of figures is that they are integrated in the document and any alteration can be made instantly without making another snapshot from Cadence. Large block diagrams become much clearer if they are drawn directly in Word as a Word-draw picture.

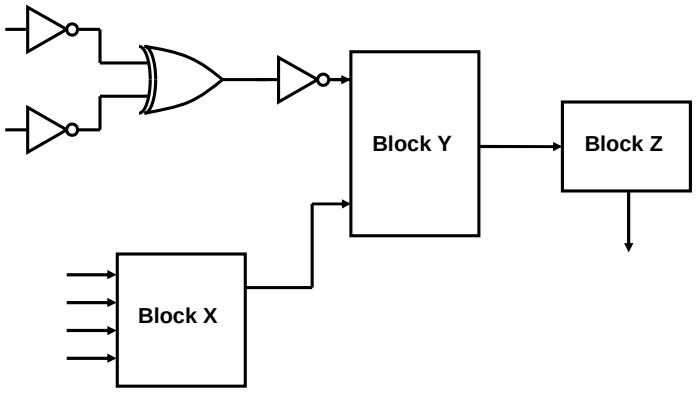



**Figure 4-3: An example of a block schematic drawn in *MS Word* with the draw function.**

## *4.5.2 How to Convert a Simulation Graph from Cadence to the Report*

Simulation results are a very important part of the status and project reports. It is imperative that the results are presented in a clear and precise way. The tool used for simulations in this project course is Spectre, included in Cadence. Cadence has a graphical user interface that presents the simulation results on the screen. There are a number of ways that one can get the graphs from Cadence to a document. In Figure 4-4 two examples are shown. Figure 4-4 shows a plot that has been printed to a PostScript file from Cadence and then translated to a TIFF file and inserted in Word. In Figure 4-4b the same plot has been taken directly from Cadence by using

snapshot. Figure 4-4a is somewhat more clear and should be considered the recommended way to extract simulation results. The snapshot function might be a good tool to use if one inverts the colors of the graphs like described in section 4.5.1. The resulting plot will then more or less be like Figure 4-4a.

A third way to get plots into a document is to export the data from Cadence to a text file. This file can then be read into Excel or MATLAB and plotted in there instead. Data can be exported to a text file by typing the following command in the *icfb* window:

```
ocnPrint(VT("/clk") ?output "./clk.txt" ?numberNotation 'none)
```

This yields a text file called *clk.txt* in the Cadence startup directory, which includes the time and voltage vectors for the voltage signal *clk*. *VT("/signal")* gets the voltage transient results of the desired signal.

Another important thing to consider when including simulation results is if they are relevant. A plot that shows a 100 MHz clock signal simulated for 2000 ns will not help much (shown in Figure 4-5). Instead zoom in to the interesting parts of the signal plots (shown in Figure 4-6).

## 4.5.3 How to Include Layouts in the Report

Including layout pictures of important blocks might be illustrative in some cases. To get good layout pictures requires some additional work. Simply taking a snapshot and adding the picture to Word might give a picture that is difficult to print. Usually the best results are reached if the picture taken from the snapshot tool is inverted so that the background is white instead of black. An alternative is to print the complete layout of a cell to a PostScript file from Cadence. These Postscripts files tend to be extremely large because they include all polygons in the layouts. To get a smaller file, convert it to a bitmap picture file (e.g. TIFF, GIF, and JPEG) by using for instance the program GIMP in UNIX.

An example of a layout plot generated like this is shown in Figure 4-7.

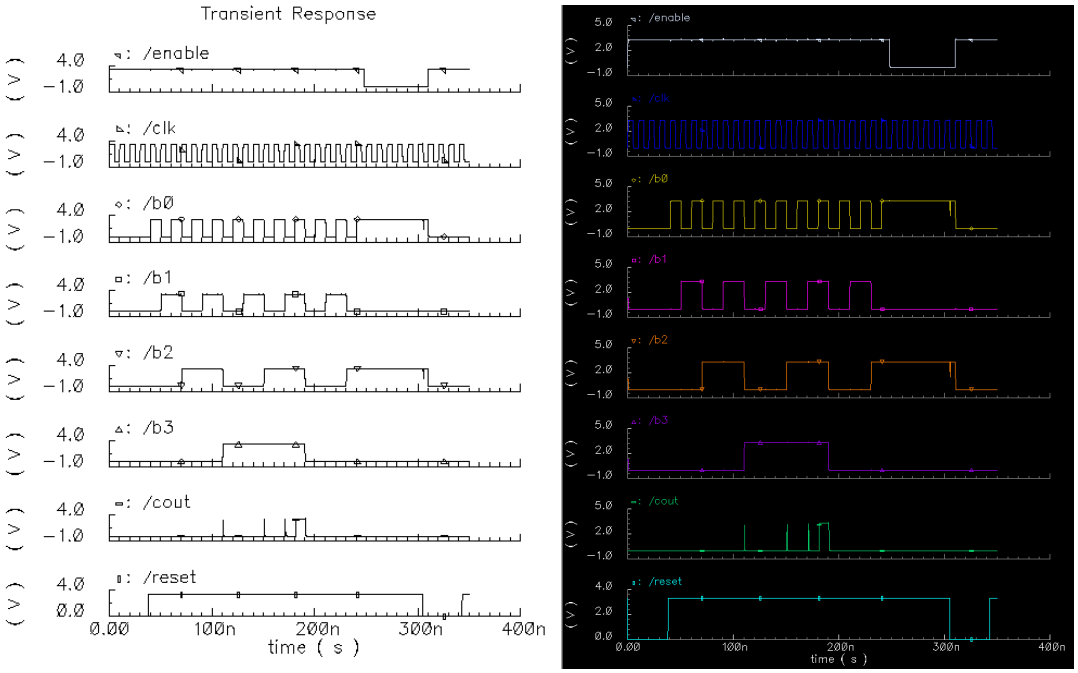



**Figure 4-4: a) Plot printed directly from Cadence with hardcopy. b) Plot taken from Cadence with snapshot.**

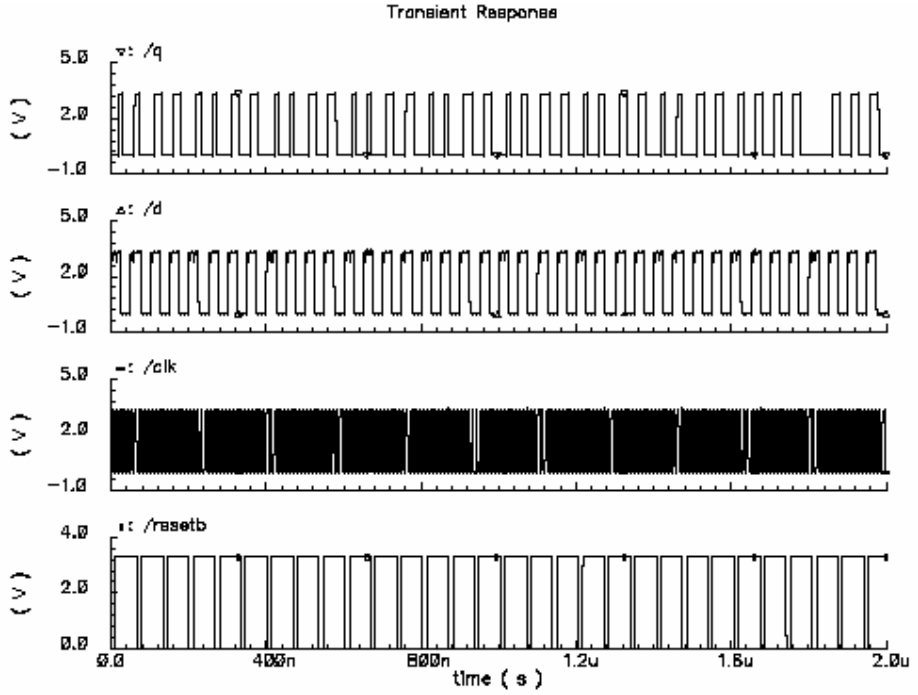



**Figure 4-5: A simulation plot that is not zoomed in.**

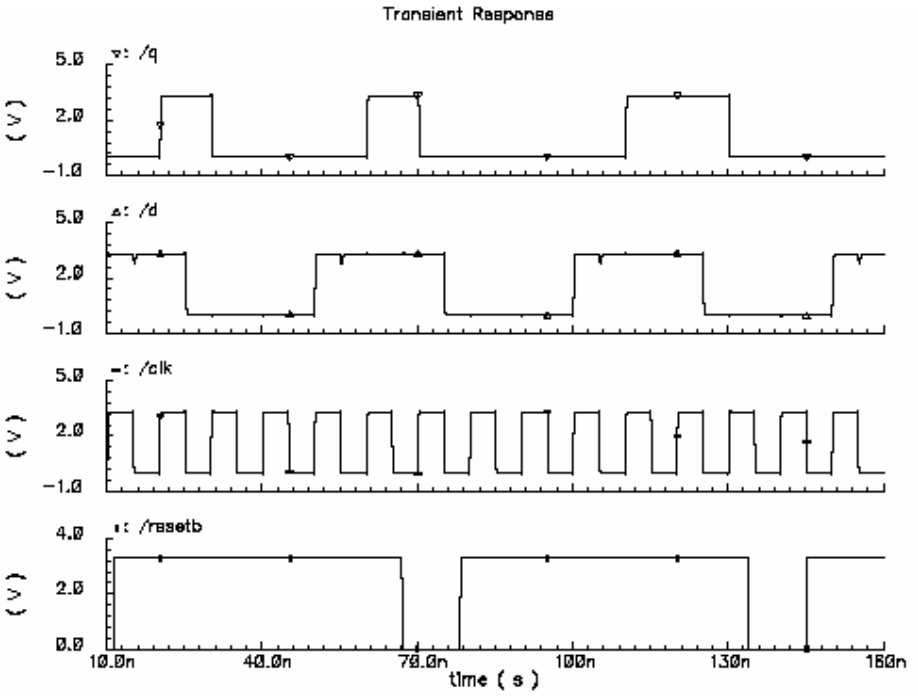



**Figure 4-6: A simulation plot that is zoomed in.**

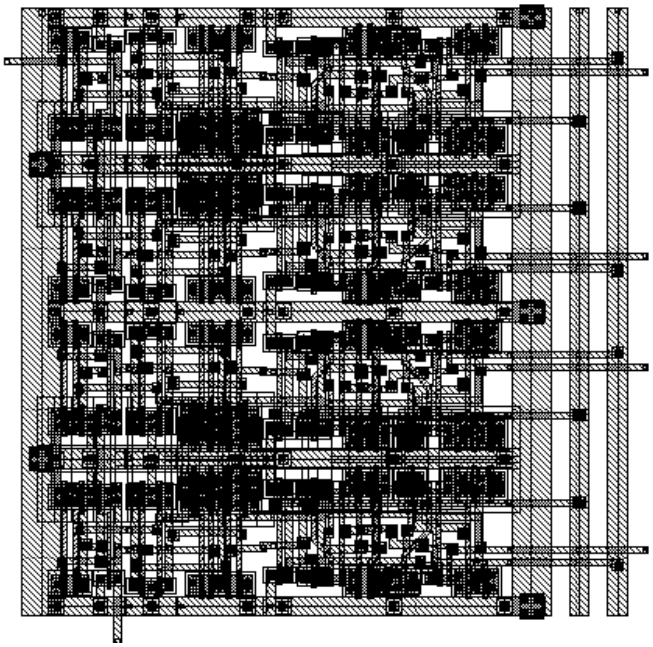


**Figure 4-7: Layout plot printed from Cadence and transformed to TIFF.**

# 5 Milestones and Tollgates

We have defined a few milestones in order to make the project more structured, and help the sponsor to keep track on the project progress. Along the project, there are certain actions that have to be completed in order to continue with the next phase. For these occasions we have tollgates that the project has to pass. The project group has passed these tollgates when the sponsor has signed the checklist for each tollgate. Completed lab-series and passing tollgate 3 are needed in order to pass the course TSEK06. Passing tollgate 4 means the student has passed the course TSEK11.

## *5.1 Definitions*

### *5.1.1 Tollgates*

A tollgate is formal decision point where the sponsor decides if the project should continue. A tollgate is not passed until the sponsor sign the appropriate checklist. In order to pass a tollgate, the project needs to supply relevant information to the sponsor, e.g. a status report as described in section 4. The sponsor might decide that a tollgate is passed with minor tasks incomplete. These uncompleted tasks have to be documented and checked at later meetings with the sponsor.

### *5.1.2 Milestones*

A milestone represents a significant achievement in the project. The ability to achieve the milestones is the basis for a good quality of the project. This structure gives the sponsor an effective way to keep track of the project progress. What should be completed at each milestone is defined by a checklist that should be passed before moving on to the next milestone. The checklists are there to help the project member to keep track on resources used on different parts of the project. The milestones will not be signed off by the sponsor.

## 5.2 Project Tollgates and Milestones

The following tollgates and milestones have been defined for the projects in this course.

### 5.2.1 Milestone 0, Project Structure

To complete this milestone the project group needs to understand what circuit to design and have an idea of how to implement the design.

The following tasks have to be completed:

1. **Project specification understood:**
   All project members must know what requirements the final chip should fulfill and what they mean.
2. **Literature study:**
   It is very likely that the problem your chip will try to solve has been solved before, at least partly. Has the project group studied literature to find ways to solve the problem?
3. **Time plan:**
   It is very useful to have a preliminary time plan that specifies how much time the project members will spend on different parts of the project. This way the project members will have a chance to notice impossible time plans at an early stage. See section 6.2 for hints on how to do the time plan.
4. **Overall design structure:**
   Based on the literature study and previous experience, the project needs to come up with a structure that has the potential to fulfill the requirement specification. Most problems can be solved in different ways. If you have found more than one way to solve the problem, you might go on and make a high level structure of more than one of them. It is a good idea to discuss the structure with your supervisor.

### 5.2.2 Tollgate 1 / Milestone 1, High-Level Design Description

To complete this milestone the project has to have a high level description of the chip.

1. **Block level description:**
   All blocks that are needed to make the chip function need to be implemented in a high level model (Verilog-A or MATLAB etc).
2. **Functionality verified through high-level simulations:**
   The high level blocks are simulated together. The simulations should verify that the blocks perform the task specified in the specification.
3. **Specification for each sub-block developed:**
   From the simulations of the high level models, you need to extract a specification for each sub block. Try to specify as many parameters as possible, try to specify what the interface between blocks should look like and how they should function. With a high quality block specification each block can be designed separately. The better the specification, the higher the chance that the blocks will function together when put together.
4. **Test-bench:**
   It is much easier to verify simulations and your design if you have good test-benches. Try to make test-benches that verify that your design works according to you design specification.
5. **Blocks assigned amongst the project members:**
   All project members (including the project leader) should after the course have had hands-on experience of design, layout and assembly of an integrated circuit.
6. **Time plan updated:**
   Is the time plan you have up to date? Did you use the estimated time for the tasks you have done so far. If not, is the time plan realistic for the things to come?
7. **Status report completed:**
   Your sponsor needs to know that the project is on track. Moreover, your supervisor also wants to know how you plan to fulfill the specifications. This way the supervisor can give the group advice and redirect and/or suggest alternative solutions to the problem if the group has chosen an unrealistic solution.

8. **Changes in specifications approved and documented:**
   Specifications are almost never static. If some part of the specification is very hard to fulfill, the project group need to discuss the possibility to make changes to the specification with the sponsor. Some specifications might be hard to evaluate and simulate and are therefore hard to verify Changes to the specification need to be approved by the sponsor. It is the sponsor that orders the project and he needs to know what the outcome of the project will be.

9. **Risks identified and documented:**
   There are always issues that can jeopardize a project. It is important for the sponsor to have a feeling of how risky the project is. To point out risks with the project to the sponsor can be a good way to start a discussion about making changes in the project. Example of risks can be a to tight time plan, lack of resources, and that blocks might not work because of too tough specifications etc.

### *5.2.3 Milestone 2, Block Design on Transistor Level*

1. **All blocks designed and simulated on transistor level:**
   Schematics for all blocks in the design have been implemented at transistor level. Test-benches exist and are functional.

2. **Blocks verified according to block specifications:**
   All blocks have been simulated and verified. Performances are according to the specifications of each block.

3. **Blocks verified at all corners specified in design specification:**
   All blocks have been simulated and function according to specification in all transistor corners, temperatures, and supply voltages that are specified in the design specification.

4. **Blocks verified under valid interface conditions:**
   To form a complete chip, the sub blocks have to be connected together. If the interfaces between blocks are not taken into account when designing sub-blocks, it is very likely that they will not function as planned when put together. For example, a clock buffer output will not have the expected rise and fall time if it has not been simulated with the correct load. A current mirror output will only have the expected output current if the correct load impedance has been used in the design work. The propagation delay of a logic gate depends on the rise and fall time of its inputs and the output rise and fall times depend on the load. To have realistic interface conditions are especially important for blocks that send high-speed signals off chip.

5. **No variables used for transistors, resistors, and capacitors:**
   To use variables in a test-bench to sweep parameters can make life simpler when designing. Using variables for transistors, resistors and capacitors will cause problems due to limitations in the design kit we use in this course. Schematic variables will result in simulations without correct parasitics, which will make your simulation results inaccurate. The specification shall be fulfilled with no variables for transistors, resistors and capacitors in the schematic. Variables in the Schematic will also cause problems during LVS. You need to have schematics free from variables before you start to create layouts of the schematic.

6. **High current nodes identified and documented:**
   There are no checks that will find wires with too high current densities. Too high current densities can cause failure in functionality. Finding high current nodes and wires is something that has to be done manually. Keep track of nodes, for instance, by adding text in the schematic specifying the maximum current.

7. **Devices sensitive to mismatch identified and documented:**
   Some circuits (read analog circuits) need to have devices that are electrically very similar. All transistors of the same size have identical electrical characteristics in the simulator but that is not the case in fabricated chips. These differences are called mismatch. There are layout techniques to minimize mismatched (matching). To use these techniques you need to identify transistors (and sometimes also resistors and capacitors) that need matching. Examples of devices that need to be matched are the input transistors of a differential amplifiers, current mirrors, resistor ladders and capacitors in switched capacitor filters.

8. **Time plan updated:**
   Is the time plan you have up to date? Did you use the estimated time for the tasks you have done so far. If not, is the time plan realistic for the things to come?

### 5.2.4 Tollgate 2 / Milestone 3, Chip Design on Transistor Level

1. **Specification verified across corners, temperature, and supply range:**
   The complete system should be simulated and function according to the design specification in all specified transistor corners, temperatures, and supply voltages.

2. **Schematic possible to use for LVS check (parallel transistors etc.):**
   Some features that are useful when designing on transistor level are not supported by the LVS tool. For instance simulating variables, ideal components, and transistor stripes.

3. **Test nodes:**
   You can observe all currents and voltages when you are running the simulator. When the chip is manufactured, you can only observe signals connected to PADs. You need to think of which nodes that you want to be able to observe on the chip. Identify potential test nodes. The number of available PADs is limited so we recommend you to choose nodes that tell you as much as possible about the circuit, which block that cause problems etc.

4. **Test-bench updated:**
   You have probably made some changes to the structure and interface of the chip since the high-level design. Do you still have test-benches that verify that your design works according to you design specification?

5. **PAD-list completed:**
   The number of pads available to the project is limited. If you have a list of all the pads that you want to use, you can check that you have enough PADs available to make your design work. You should also make sure that you have enough signals off-chip to be able to find what the problem is if the chip does not work after fabrication.

6. **Verification plan:**
   With the limited number of pads available, you need to think of how you should be able to verify that the manufactured chip works according to the specification. To make sure that the measurements you want to do can be done with the equipment we have available in the lab, we need to have a rough idea about what you want to do.

7. **High-current nodes identified and documented:**
   You will have the same current issues you had in the separate blocks when these are connected together. Make sure you have identified high current nodes at the top level of the design. This is good to know when you connect the individual blocks into a chip layout.

8. **Mismatch sensitive devices/parts identified and documented:**
   See Milestone 2, Block Design on Transistor Level point 7.

9. **Changes in specification approved, verified, and documented:**
   See Tollgate 1 / Milestone 1, High-Level Design Description point 8.

10. **Risks identified and documented:**
    See Tollgate 1 / Milestone 1, High-Level Design Description point 9.

11. **Milestone 1-2 passed?**
    The checklist for milestone 3 does not include all tasks for milestone 1 and 2. We presume that all tasks for the previous milestones are done.

12. **Time plan updated?**
    See Tollgate 1 / Milestone 1, High-Level Design Description point 6.

13. **Status report completed?**
    See Tollgate 1 / Milestone 1, High-Level Design Description point 7.

### 5.2.5 Milestone 4, Block Design Layout

1. **All blocks DRC clean (switches: no_coverage, no_generated_layers, and grid (min. 0.025)):**
   The manufacturer of the chips cannot manufacture designs with DRC errors. Your layout blocks need to be free of DRC errors. Not all DRC checks are applicable for individual blocks; some are only valid for the whole chip. You can therefore run your DRC checks with the following switches and only with these switches: *"no_coverage, no_generated_layers, grid"* (make sure the grid setting is 0.025!).
2. **All blocks LVS clean?**
   If you do not want to spend weeks to find errors in the layout at the top level you need to make sure all sub blocks are correct.
3. **All blocks verified according to block specification:**
   The best way to verify that your design works according to the specification is to simulate the complete chip with all extracted layout parasites. Usually this is not possible, because the computers are not fast enough. The second best is to verify that the sub blocks work according to the specification with layout parasitics.
4. **Blocks simulated under valid interface conditions:**
   You cannot trust the simulation results if you have not modeled the interfaces correctly.
5. **Wide enough wires for high current nodes:**
   Have the layout of nodes that are identified as high current nodes been made in a way that ensures that the maximum current density for wires is not exceeded?
6. **Careful layout of mismatch sensitive devices:**
   Have the layout of devices that are sensitive to mismatch been made in such a way that mismatch is minimized?
7. **Floor plan and routing strategies discussed and documented:**
   When you have the layout of the individual blocks, you can start to think of how to place them on the chip. How to minimize wire lengths for high speed or sensitive signals or high current wires? How to make routing simple?
8. **Total core area estimated (fits in assigned area?):**
   There is a problem if the area needed by the design is larger the available area. You need to discuss area issues with your supervisor. Is there a possibility to get area from another project or do you need to exclude parts of your design?
9. **PAD frame designed:**
   One block that will be in every project is the PAD frame. Do not forget to make the layout of that block.
10. **PAD frame DRC and clean:**
    There are usually some special tricks needed to get the PAD frame through LVS and DRC. You will find that information in the lab manual [4].
11. **Risks identified and documented:**
    See Tollgate 1 / Milestone 1, High-Level Design Description point 9.
12. **Time plan updated:**
    See Tollgate 1 / Milestone 1, High-Level Design Description point 6.

### 5.2.6 Milestone 5, Chip Assembly

1. **Chip core assembled:**
   Are all parts except the pad frame, and filling connected together?
2. **Chip core DRC clean (switches: no_coverage, no_generated_layers):**
   Have you run a DRC check of the finished core layout with and only with the switches: *"no_coverage no_generated_layers, grid"*. Did the core design pass the DRC run with no errors?
3. **Chip core LVS clean:**
   Do the layout and schematic match for the core layout?
4. **LVS schematic (or analog_extracted view) verified through functional test:**
   During the layout process, it is very likely that you have made some changes to the schematic. For

instance change the hierarchy of the schematic to match the layout, added decoupling and dummy structures to the schematic to get a clean LVS run. You need to verify that you have the correct functionality after these small changes. If possible simulate an *analog_extracted* view of the core and verify that the chip functions as expected. If this is unrealistic, simulate exactly the schematic that was used for LVS.

5. **Decoupling capacitors added (both in layout and schematic):**
   It is absolutely crucial to have decoupling capacitors on-chip. The bond-wire inductance will cause the on-chip power supply voltage to be unstable if decoupling capacitances are not used. The high frequency switching of logic blocks will see a high impedance in the bond wires, which will cause a drop in supply voltage. Hopefully your design will not occupy the entire available core area. It is highly recommend that you fill all extra space with decoupling capacitors.

6. **Wide enough wires for high current nodes**
   See Milestone 4, Block Design Layout point 5.

7. **Chip including PAD frame, decaps., and core DRC and LVS clean:**
   The complete chip including PAD frame and decoupling capacitors should be DRC and LVS clean. The DRC should be run with only the "*no_generated_layers*" switch set. If you find DRC errors that relate to coverage rules, you need to run fill scripts to remove these errors. This is not required until Tollgate 3 / Milestone 6.

8. **Risks identified and documented:**
   See Tollgate 1 / Milestone 1, High-Level Design Description point 9.

9. **Time plan updated:**
   See Tollgate 1 / Milestone 1, High-Level Design Description point 6.

### *5.2.7 Tollgate 3 / Milestone 6, Tape Out*

1. **Pattern fills generated and added:**
   The field implant layer needs to be included in the layout. This is done by running a script. The field implant layer will minimize the risk of parasitic p-MOS transistors between Poly-interconnect and the substrate.

2. **Complete chip layout DRC and LVS clean:**
   DRC OK without any switches and LVS OK for the total chip

3. **GDS file generated:**
   The manufacturer needs a GDS file to make the chip. You need to generate this file.

4. **Specification changes approved by sponsor and documented:**
   See Milestone 2, Block Design on Transistor Level.

5. **Test-bench updated:**
   See Milestone 4, Block Design Layout.

6. **PAD-list completed:**
   See Milestone 4, Block Design Layout.

7. **Verification plan:**
   See Milestone 4, Block Design Layout.

8. **Schematic of peripheral components:**
   When you do your simulations you know how the chip should be connected. After the summer you will probably have forgotten some details. The final project report should include a sketch of how the chip should be connected during verification. The schematic should include the chip and peripheral components needed for the evaluation. We recommend that the report also includes a list of values you expect to measure at your PADs. This way you can compare the measurements and simulations to find discrepancies and identify malfunction.

9. **Identified risks documented and discussed:**
   See Tollgate 2 / Milestone 3, Chip Design on Transistor Level

10. **Milestone 1-5 passed:**
    The checklist for milestone 6 does not include all tasks for milestone 1 through 5. We presume that all tasks for the previous milestones are done.

11. **Final project report completed:**
    To complete the project you need to deliver both the GDS file and documentation. The final report should give the sponsor the possibility to know what the project has accomplished.

12. **Presentation completed:**
    A part of the examination of the course is to present you project to the other attendees of the course. This should be done as a roughly 10 minute long presentation.

13. **Project feedback:**
    The supervisors and the course responsible are very interested in your opinion about the course. How can we improve the course, what was good, what parts need improvements? Take the opportunity to reflect on the project. What were the good parts, what parts did not turn out so good? What would you change if you would do the project again?

### *5.2.8 Milestone 7, Measurement Plan*

1. **What to measure?**
   You have a limited amount of time and equipment to do your chip evaluation. What do you want to measure on your chip? Will these measurements validate that you chip performance according to the design specification?

2. **How to measure?**
   In the simulator you can sense what ever you want. In the lab you are more limited. How will you get measurements values?

3. **PCB schematic:**
   What should your evaluation PCB look like? Which components do you need? How should they be connected together?

4. **PCB component list:**
   Which components are needed for your PCB? We probably need to buy some of them before you can start measuring.

5. **Necessary instruments available:**
   We do not have all kinds of instruments in the lab. Are the instruments you need for your measurements available? Do they have the performance you need?

6. **Lab booked for soldering:**
   There is only one soldering station available for the course. Have you booked a time for your group?

7. **Soldered PCB checked for shorts and opens:**
   Before you connect your chip to the PCB, make sure to check your PCB for shorts and openings. We have had too many examples of burned chips caused by errors in the PCB.

8. **Lab booked for measurements:**
   The amount of measurement equipment is limited. Have you booked all equipment you need to complete your evaluation?

### *5.2.9 Tollgate 4 / Milestone 8, Chip Evaluation*

1. **Measurement results documented:**
   What have you measured and what were the results?

2. **Measurements compared to simulation results:**
   It will give you great feedback to compare the simulation results you had during the design of the chip and the measured results. Are they similar? What differences have you found? Do you have any idea about why you have found differences?

3. **Evaluation presentation:**
   A part of the examination of the course is to present you results to the other attendees of the course. This should be done as a roughly 10 minute long presentation.

4. **Evaluation report:**
   The results from the measurements should be presented in a report.

# 6 Time Plan

## 6.1 Activities

**IN TABLE 6-1 BELOW ARE SOME OF THE ACTIVITIES THAT ARE RECOMMENDED TO HAVE IN THE TIME PLAN FOR TOLLGATE 1-3 (TSEK06). AN EXAMPLE OF A TIME PLAN IS SHOWN IN**
Table 6-2.

**TABLE 6-1: LIST OF BASIC ACTIVITIES IN THE PROJECT.**

| Nr | Activities | Description |
|---|---|---|
| 1 | Time plan | Make time plan and keep it up to date |
| 2 | Pre-study | Litterateur search, find good potential implementation structures. |
| 3 | High level modeling | Create a high level model for a design that functions according to the specification |
| 4 | Status report for TG1 | Write the report |
| 5 | Transistor block design | Create schematics of all blocks and verify that they work according to specification. |
| 6 | Chip designs on transistor level | Complete schematic of chip and chip verification |
| 7 | Status report for TG2 | Write the report |
| 8 | Block layout and verification | Make block layout and verify through LVS and DRC. |
| 9 | PAD frame | Layout and decide which pads to use, DRC and LVS. |
| 10 | Chip core layout | Global place and route, DRC, LVS, verification. |
| 11 | Generate fill and additional layers and Tape-Out | Stream out and run the needed scripts (see [4]). |
| 12 | Verification plan | Decide what should be measured and how. |
| 13 | Project report | Write the report |
| 14 | Project presentation | Prepare and present your results to your course colleagues. |

## 6.2 Time Plan Recommendations

We do not expect you to make a perfect time plan the first time. As the project proceeds, you will need to update the time plan. However, a rough time plan is required at the beginning of the project to make sure that there are resources available for all parts. The project part of the course TSEK06 gives 7.5 credits of the total 12 credits. Based on experience from previous projects in this course, a rough resource allocation can be summarized as:

- High-Level deigns and design topology 10-20%
- Transistor level design and verification 30-40%
- Layout level and chip assembly 40-60%

Do not start late. If you fail to complete a step in the design schedule on time, catch up with the work as soon as possible. If not, there will soon be another deadline and you will be very late.

### 6.2.1 Recommended Tollgates Dates

In order for the project to flow and to increase the chance of success, recommended dates for the different tollgates are specified in the project specification. The deadline for tollgate 3 is set in order to give the supervisors time to put the projects together to a chip and send it to the chip vendor before the tape-out deadline. The deadline for the third tollgate should therefore be considered as a very hard deadline. The other tollgates have more dynamic deadline dates. However, each group needs to come with a good and well motivated explanation in order to change the tollgate dates substantially.

As this course does not have any written exam, the requirements for the projects are harder. Consider tollgate 3 deadline as a written exam. If you show up one day too late for a written exam, you will fail that course.

**TABLE 6-2: TIME PLAN EXAMPLE.**

| Planning | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Project:** | **32 bit High-Performance Low-Power ALU** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Project group:** | Group 1 | | **Date:** | | | | | | | | | | | | **Reviewed:** | | | | | | | | | | | | | | | | | |
| **Customer:** | | | **Version:** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Course:** | TSEK06 VLSI Design Project | | **Author:** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **ACTIVITIES** | | **TIME** | **WHO** | **TIME PLAN (week number)** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| no | Description | hours | Initials | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | | | | | | | |
| 1 | pre-study | | all | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | make a timeplan | | aa | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | high-level modeling | | bb,cc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | status report for TG 1 | | dd | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | transistor block design | | aa,bb,dd | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | chip design on transistor level | | cc | | | | | | | | | E | | | | H | E | | | | | | E | E | H | | | | | | | |
| 7 | status report for TG 2 | | dd | | | | | | | | | X | | | | O | X | | | | | | X | X | O | | | | | | | |
| 8 | block layout and verification | | aa,bb,dd | | | | | | | | | A | | | | L | A | | | | | | A | A | L | | | | | | | |
| 9 | PAD-frame | | cc | | | | | | | | | M | | | | I | M | | | | | | M | M | I | | | | | | | |
| 10 | chip core layout | | bb,cc | | | | | | | | | I | | | | D | I | | | | | | I | I | D | | | | | | | |
| 11 | generate fill and additional layers | | cc | | | | | | | | | N | | | | A | N | | | | | | N | N | A | | | | | | | |
| 12 | tapeout | | aa,bb,cc | | | | | | | | | A | | | | Y | A | | | | | | A | A | Y | | | | | | | |
| 13 | verification plan | | dd | | | | | | | | | T | | | | S | T | | | | | | T | T | S | | | | | | | |
| 14 | project report | | dd | | | | | | | | | I | | | | | I | | | | | | I | I | | | | | | | | |
| 15 | project presentation | | aa,bb | | | | | | | | | O | | | | | O | | | | | | O | O | | | | | | | | |
| 16 | milestone 0 | | | | fr | | | | | | | N | | | | | N | | | | | | N | N | | | | | | | | |
| 17 | milestone 1 | | | | | | fr | | | | | | | | | | | | | | | | | | | | | | | | | |
| 18 | milestone 2 | | | | | | | | | fr | | P | | | | | P | | | | | | P | P | | | | | | | | |
| 19 | milestone 3 | | | | | | | | | | fr | E | | | | | E | | | | | | E | E | | | | | | | | |
| 20 | milestone 4 | | | | | | | | | | | R | | | | | R | mo | | | | | R | R | | | | | | | | |
| 21 | milestone 5 | | | | | | | | | | | I | | | | | I | | | fr | | | I | I | | | | | | | | |
| 22 | milestone 6 | | | | | | | | | | | O | | | | | O | | | | | we | O | O | | | | | | | | |
| 23 | | | | | | | | | | | | D | | | | | D | | | | | | D | D | | | | | | | | |
| 24 | tollgate 1 | | all | | | | fr | | | | | | | | | | | | | | | | | | | | | | | | | |
| 25 | tollgate 2 | | all | | | | | | | | fr | | | | | | | | | | | | | | | | | | | | | |
| 26 | tollgate 3 | | all | | | | | | | | | | | | | | | | | | | we | | | | | | | | | | |
| | Sum, number of hours | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

### *6.2.2 Recommended Milestone Dates*

Dates for the milestones – the different steps in the VLSI design methodology – should be decided on together with the supervisor of the respective group. Guidelines to some of these dates are printed in the project specification.

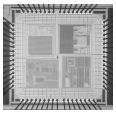
# 7 References

[1]. Svensson Tomas, and Krysander Christian, **LIPS – nivå 1**, Version 1, Bokakademin, Linköping University, 2002.

[2]. Weste Neil H. E., and Kamran Eshraghian, **Principles of CMOS VLSI Design – A system perspective**, Second edition, Addison-Wesley, 1993, *ISBN 0-201-53376-6.*

[3]. Rabaey Jan M., Chandrakasan Anantha, and Nikolic Borivoje, **Digital Integrated Circuits – A design perspective**, Second edition, Prentice Hall, 2003, *ISBN 0-13-120764-4.*

[4]. Daniel Svärd and Atila Alvandpour, **TSEK06 VLSI Chip Design Project 2011**, Fifth edition, Bokakademin, Linköping University, 2011



# Check List for Milestone 0

## Project Structure and Definition

**Project Group Members:** _____

_____

**Milestone:**

[ ] – Passed
[ ] – Passed with incomplete tasks
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | Project specification understood | |
| 2 | Literature study | |
| 3 | Time plan | |
| 4 | Overall design structure | |

Notes and incomplete tasks

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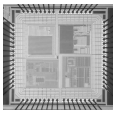

# Check List for Tollgate 1 / Milestone 1

## High-Level Description and Design

**Project Group Members:** _____

_____

**Tollgate:**

[ ] - Passed
[ ] - Passed with incomplete tasks
[ ] - Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | Block level description | |
| 2 | Functionality verified through high-level simulations | |
| 3 | Specification for each sub-block developed | |
| 4 | Test-bench | |
| 5 | Block assigned amongst the project members | |
| 6 | Time plan updated | |
| 7 | Status report completed | |
| 8 | Changes in specifications approved and documented | |
| 9 | Risks identified and documented | |

Notes and incomplete tasks

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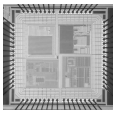
**Sponsor signature:** _____



# Check List for Milestone 2

## Block Design on Transistor Level

**Project Group Members:** _____

_____

**Milestone:**

[ ] – Passed
[ ] – Passed with incomplete tasks
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | All blocks designed and simulated on transistor level | |
| 2 | Blocks verified according to block specifications | |
| 3 | Blocks verified at all corners specified in design specification | |
| 4 | Blocks verified under valid interface conditions | |
| 5 | No variables used for transistors, resistors, and capacitors | |
| 6 | High current nodes identified and documented | |
| 7 | Devices sensitive to mismatch identified and documented | |
| 8 | Time plan updated | |

Notes and incomplete tasks

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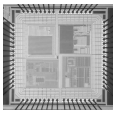

# Check List for Tollgate 2 / Milestone 3

## Chip Design on Transistor Level

**Project Group Members:** _____

_____

**Tollgate:** [ ] – Passed
[ ] – Passed with incomplete tasks
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomplete) |
|---|---|---|
| 1 | Specification verified across corners, temperature, and supply range | |
| 2 | Schematic possible to use for LVS check (parallel transistors etc.) | |
| 3 | Test nodes | |
| 4 | Test-bench updated | |
| 5 | PAD-list completed | |
| 6 | Verification plan | |
| 7 | High-current nodes identified and documented | |
| 8 | Mismatch sensitive devices/parts identified and documented | |
| 9 | Changes in specification approved, verified, and documented | |
| 10 | Risks identified and documented | |
| 11 | Milestone 1-3 passed | |
| 12 | Time plan updated | |
| 13 | Status report completed | |

Notes and incomplete tasks

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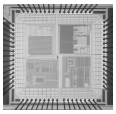
**Sponsor signature:** _____





# Check List for Milestone 4

## Block Design Layout

**Project Group Members:** _____

_____

**Milestone:**

[ ] – Passed
[ ] – Passed with incomplete tasks
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | All blocks DRC clean (switches: no_coverage, no_generated_layers, and grid (min. 0.025)) | |
| 2 | All blocks LVS clean | |
| 3 | All blocks verified according to block specification | |
| 4 | Blocks simulated under valid interface conditions | |
| 5 | Wide enough wires for high current nodes | |
| 6 | Careful layout of mismatch sensitive devices | |
| 7 | Floor plan and routing strategies discussed and documented | |
| 8 | Total core area estimated (fits in assigned area?) | |
| 9 | PAD frame designed | |
| 10 | PAD frame DRC and LVS clean | |
| 11 | Risks identified and documented | |
| 12 | Time plan updated | |

Notes and incomplete tasks

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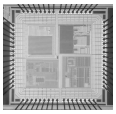

# Check List for Milestone 5

## Chip Assembly

**Project Group Members:** _____

_____

**Milestone:**

[ ] – Passed
[ ] – Passed with incomplete tasks
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomplete) |
|---|---|---|
| 1 | Chip core assembled | |
| 2 | Chip core DRC clean (switches: no_coverage, no_generated_layers) | |
| 3 | Chip core LVS clean | |
| 4 | LVS schematic (or analog_extracted view) verified through functional test | |
| 5 | Decoupling capacitors added (both in layout and schematic) | |
| 6 | Wide enough wires for high current nodes | |
| 7 | Chip including PAD frame, decaps., and core DRC and LVS clean | |
| 8 | Risks identified and documented | |
| 9 | Time plan updated | |

Notes and incomplete tasks

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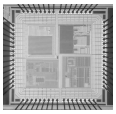

# Check List for Tollgate 3 / Milestone 6

## Tape Out

**Project Group Members:** _____

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**Tollgate:** [ ] – Passed (on project in TSEK01)
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | Pattern fills generated and added | |
| 2 | Complete chip layout DRC and LVS clean | |
| 3 | GDS file generated | |
| 4 | Specification changes approved by sponsor and documented | |
| 5 | Test-bench updated | |
| 6 | PAD-list completed | |
| 7 | Verification plan | |
| 8 | Schematic of peripheral components | |
| 9 | Identified risks documented and discussed | |
| 10 | Milestone 1-5 passed | |
| 11 | Final project report completed | |
| 12 | Presentation completed | |
| 13 | Project feedback | |

Notes and incomplete tasks

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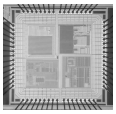
**Sponsor signature:** _____



# Check List for Milestone 7

## Measurement Plan

**Project Group Members:** _____

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**Milestone:**

[ ] – Passed
[ ] – Passed with incomplete tasks
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | What to measure? | |
| 2 | How to measure? | |
| 3 | PCB schematic | |
| 4 | PCB component list | |
| 5 | Necessary instruments available | |
| 6 | Lab booked for soldering | |
| 7 | Soldered PCB checked for shorts and opens | |
| 8 | Lab booked for measurements | |

Notes and incomplete tasks

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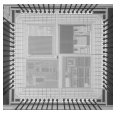

# Check List for Tollgate 4 / Milestone 8

## Chip Evaluation

**Project Group Members:** _____

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**Tollgate:** [ ] – Passed (on TSEK11)
[ ] – Failed

Check list

| Nr | Description | Completed (Y/N/Incomp.) |
|---|---|---|
| 1 | Chip evaluation | |
| 2 | Measurement results documented | |
| 3 | Measurements compared to simulation results | |
| 4 | Evaluation presentation | |
| 5 | Evaluation report | |

Notes and incomplete tasks

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**Sponsor signature:** _____