Solutions to Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	August 25, 2003
Time:	14 – 18
Max. no of points:	70; 50 from written test, 5 for the project, and 15 for the assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The circuit shown in Figure 1.1(a) can be a part of an opamp. In this exercise neglect the channel-length modulation.

a) Determine the output voltage, V_{out}, as a function of the input voltage, V_{in}, for the circuit shown in Figure 1.1(a). Assume that both transistors are saturated.

The current through a transistor operating in the saturation region is given by

$$I_D = \alpha(V_{GS} - V_{TH})^2 \tag{1.1}$$

if the channel-length modulation is neglected. For the transistors M_1 and M_2 the current should be equal according to KCL. Hence,

$$I_{D1} = \alpha_1(V_{in} - V_{bias} - V_{TH1})^2 = \alpha_2(V_{out} - V_{TH2})^2 = I_{D2} \tag{1.2}$$

Solving for V_{out} yields

$$V_{out} = \sqrt{\frac{\alpha_1}{\alpha_2}}(V_{in} - V_{bias} - V_{TH1}) + V_{TH2} \tag{1.3}$$

which is the answer for this exercise.

b) Determine the DC gain of the circuit by using large-signal analysis. The transistors are operating in the saturation region.

The DC gain is derived as the derivative of the output voltage with respect to the input voltage when they are expressed in terms of large-signal quantities as in (1.3). Hence,

$$\frac{dV_{out}}{dV_{in}} = \sqrt{\frac{\alpha_1}{\alpha_2}} \tag{1.4}$$

the only way to increase the DC gain is to increase the size of the PMOS transistor and decrease the size of the NMOS transistor. This is for a first-order approximation of the performance of the circuit.

c) Assume that transistor M_2 is replaced by a resistor, R, as is shown in Figure 1.1(b). Determine the output voltage as a function of the input voltage, $V_{out} = f(V_{in})$. The input voltage ranges from zero to large input voltages, e.g., $V_{in} » V_{bias}$. In the graph denote the operation regions of transistor M_1.

For small input voltages below $V_{bias} + V_{TH1}$ the transistor is operating in the cut-off region. This means that the current through transistor M_1 is very small and can be considered zero. Hence, no voltage drop over the resistor replacing M_2 is the result which leads to zero volt at the output node.

Increasing the voltage above $V_{bias} + V_{TH1}$ results in a source-gate minus the threshold voltage smaller than the source-drain voltage and the transistor is operating in the saturation region. From the above analysis we know that the output voltage is linearly related to the applied input voltage. Hence, the output voltage will increase at the same rate as the input voltage.

If we increase the input voltage even further, the source-drain voltage will be smaller than the source-gate voltage minus the threshold voltage which will lead that the transistor is operating in the linear region. In the linear region the current through the device will increase slower than in the saturation region. Hence, the output voltage increase rate will start to decrease. The output voltage as a function of the input voltage is shown in Figure 1.1.

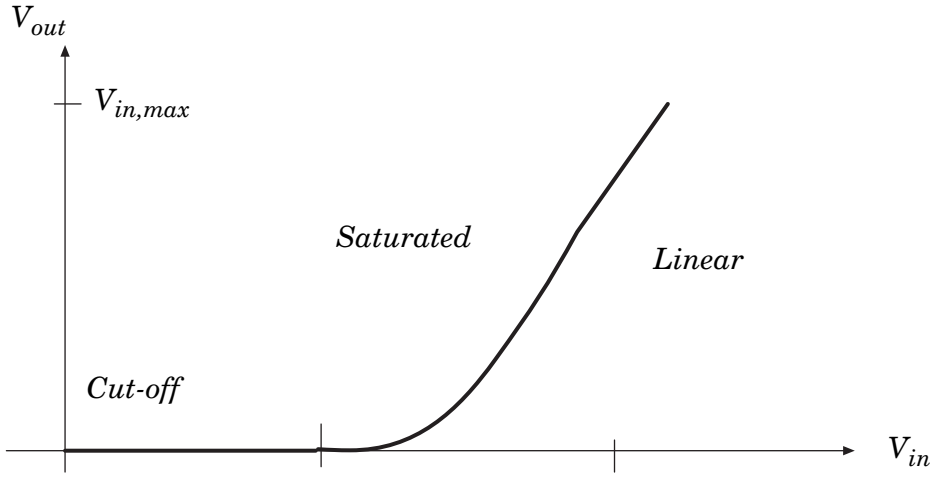

Figure 1.1 The output voltage as a function of the input voltage.

2. Small-signal analysis

A commonly used circuit in analog design is shown in Figure 2.1(a). In this exercise assume that all transistors are biased to operate in the saturation region.

a) Derive the transfer function, i.e., V_{out}/V_{in}, of the circuit shown in Figure 2.1(a). Do not neglect the bulk effects.

The small-signal model of the amplifier is shown in Figure 2.1.

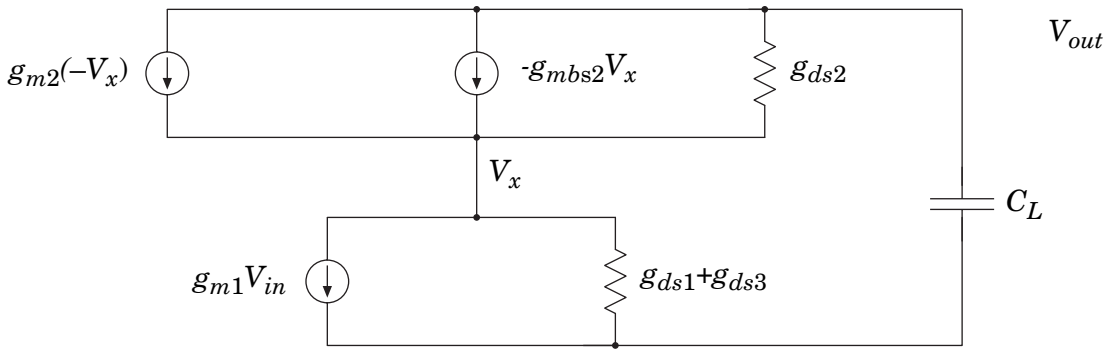

Figure 2.1 Small-signal model of the gain-boosted folded-cascode amplifier.

The transfer function can be derived by for example using nodal analysis in the nodes V_x and V_{out}.

$$g_{m1}V_{in} + V_x(g_{ds1} + g_{ds3}) + (g_{m2} + g_{mbs2})V_x + (V_x - V_{out})g_{ds2} = 0$$

$$(g_{m2} + g_{mbs2})V_x + (V_x - V_{out})g_{ds2} - V_{out}sC_L = 0$$

In the lowermost equation we can solve for V_x

$$V_x = \frac{g_{ds2} + sC_L}{g_{m2} + g_{msb2} + g_{ds2}}V_{out}. \qquad (2.1)$$

Inserting this into the other equation and some simplifications yields

$$g_{m1}V_{in} + (g_{ds1} + g_{ds3})\frac{g_{ds2} + sC_L}{g_{m2} + g_{msb2} + g_{ds2}}V_{out} + sC_LV_{out} = 0$$

which is rewritten to

$$-g_{m1}(g_{m2} + g_{msb2} + g_{ds2})V_{in} = (g_{ds1} + g_{ds3})g_{ds2} + sC_L(g_{ds1} + g_{ds3} + g_{m2} + g_{msb2} + g_{ds2}).$$

The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m2} + g_{msb2} + g_{ds2})}{(g_{ds1} + g_{ds3})g_{ds2} + sC_L(g_{ds1} + g_{ds3} + g_{m2} + g_{msb2} + g_{ds2})}$$

which is approximated to

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{(g_{ds1} + g_{ds3})g_{ds2}}{g_{m2}} + sC_L} \qquad (2.2)$$

by assuming that $g_m \gg g_{mbs}$, $g_m \gg g_{ds}$.

b) Derive expressions for the DC gain, first pole, and the unity-gain frequency in terms of I, W, and L for the circuit shown in Figure 2.1(a). Neglect the influence of the bulk effect.

The DC gain is given by

$$A_0 = \frac{g_{m1}g_{m2}}{(g_{ds1}+g_{ds3})g_{ds2}} \propto \frac{\sqrt{\frac{W_1}{L_1}(I_1+I_3)}\sqrt{\frac{W_2}{L_2}I_1}}{\left(\frac{1}{L_1}(I_1+I_3)+\frac{1}{L_3}I_3\right)\frac{1}{L_2}I_1} = \sqrt{\frac{W_1L_1}{(I_1+I_3)+\frac{L_1}{L_3}I_3}}\sqrt{\frac{W_2L_2}{I_1}}.$$

The pole is expressed as

$$p_1 \approx \frac{(g_{ds1}+g_{ds3})g_{ds2}}{g_{m2}C_L} \propto \frac{\left(\frac{1}{L_1}(I_1+I_3)+\frac{1}{L_3}I_3\right)\frac{1}{L_2}I_1}{C_L\sqrt{\frac{W_2}{L_2}I_1}} = \frac{\frac{1}{L_1}(I_1+I_3)+\frac{1}{L_3}I_3}{C_L\sqrt{\frac{W_2L_2}{I_1}}}.$$

The unity-gain frequency is approximately given by

$$\omega_u \approx A_0p_1 \approx \frac{g_{m1}g_{m2}}{(g_{ds1}+g_{ds3})g_{ds2}}\frac{(g_{ds1}+g_{ds3})g_{ds2}}{g_{m2}C_L} = \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\frac{W_1}{L_1}(I_3+I_1)}}{C_L}.$$

c) How are the DC gain, first pole, and the unity-gain frequency changed if...
... the current I_1 is increased?
... V_{bias2} is decreased?
... the channel-length of transistor M_3 is doubled?
Assume that the transistors remain saturated. Motivate your answer carefully.

If the current I_1 is increase the DC gain will decrease, the pole location will increase, and the unity-gain frequency will increase according to the expression of the exercise b.

If V_{bias} is decreased to current through transistor M_3 will increase which results in increased I_3. Hence, the DC gain will decrease, the magnitude of the pole will increase, and the unity-gain frequency will increase.

If the channel-length of the transistor M_3 is doubled the DC gain will increase, the magnitude of the pole will decrease, while the unity-gain frequency is constant.

3. Macro block level analysis

The circuit shown in Figure 3.1 is used in all active-RC leapfrog filters.

a) Derive the transfer function from the input to the output, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. Assume that the operational amplifier is ideal except that it suffers from a finite DC gain, i.e., $A(s) = A_0$. Further, what is the minimum DC gain of the opamp in order to have a maximum DC gain error smaller than ε percent for the circuit in Figure 3.1? ε is defined as Eq. (3.1) where H_{ideal} is the transfer function with an ideal opamp while $H_{finitegain}$ is the transfer function with an opamp with finite gain.

$$\varepsilon = \left| \frac{H_{ideal}(0) - H_{finitegain}(0)}{H_{ideal}(0)} \right| \tag{3.1}$$

The negative input node of the opamp is called V_x. The output voltage of the opamp is given by

$$V_{out} = A(0 - V_x) \tag{3.2}$$

which yields $V_x = -V_{out}/A$. Setting up the nodal analysis of the circuit yields

$$(V_{in} - V_x)G_1 = (V_x - V_{out})(G_2 + sC). \tag{3.3}$$

Solving for the output voltage yields

$$V_{out} = -\frac{G_1 V_{in}}{\frac{G_1}{A} + \left(1 + \frac{1}{A}\right)(G_2 + sC)} = -\frac{R_2}{R_1}\frac{V_{in}}{\frac{R_2}{R_1}\frac{1}{A} + \left(1 + \frac{1}{A}\right)(1 + sR_2C)} \tag{3.4}$$

The DC gain of the lossy integrator is ideally R_2/R_1 which is given from Eq. (3.4) by letting $A \to \infty$. The expression for the DC gain is achieved by setting $s = 0$ which results in

$$\left.\frac{V_{out}}{V_{in}}\right|_{s=0} = -\frac{R_2}{R_1}\frac{1}{\frac{R_2}{R_1}\frac{1}{A} + \left(1 + \frac{1}{A}\right)} = -\frac{R_2}{R_1}\frac{1}{1 + \left(1 + \frac{R_2}{R_1}\right)\frac{1}{A}}. \tag{3.5}$$

The error between the DC gain of an ideal opamp and the value achieved by an opamp with finite gain is

$$\left| \frac{H_{ideal}(0) - H_{finitegain}(0)}{H_{ideal}(0)} \right| = \left(1 - \frac{1}{1 + \left(1 + \frac{R_2}{R_1}\right)\frac{1}{A}} \right) \leq \varepsilon. \tag{3.6}$$

which can be simplified to

$$\varepsilon \geq \frac{1 + \frac{R_2}{R_1}}{A + 1 + \frac{R_2}{R_1}}. \tag{3.7}$$

which yields

$$A \geq \frac{1 + \frac{R_2}{R_1}}{\varepsilon} - 1 - \frac{R_2}{R_1} = \frac{1}{\varepsilon}\left(\frac{R_2}{R_1} + 1\right) - 1 - \frac{R_2}{R_1}. \tag{3.8}$$

Hence, if the maximum DC gain error should be smaller than 0.1% and $R_2 = 10R_1$ the minimum required DC gain of the opamp is 10989 times which is approximately 80.8 dB.

b) Assume instead that the amplifier is ideal except that it suffers from an offset voltage, V_{os}. Derive the output voltage as a function of the input and offset voltage. How is the output voltage affected by the offset voltage?

Performing the same analysis as in exercise a but in Eq. (3.3) replace V_x by V_{os} yields the output voltage

$$V_{out} = -\frac{G_1}{G_2 + sC}V_{in} + \left(\frac{G_1}{G_2 + sC} + 1\right)V_{os}$$

$$= -\frac{R_2}{R_1}\frac{1}{1 + sR_2C}V_{in} + \left(1 + \frac{R_2}{R_1}\frac{1}{1 + sR_2C}\right)V_{os}. \qquad (3.9)$$

Hence, the output voltage increased by the offset voltage plus the integrated offset voltage with losses.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure. The input signal is sampled according to $V_{in}(t) = V_{in}(t + \tau)$.

a) Determine the transfer function, $V_{out}(z)/V_{in}(z)$, and plot the location of the possible poles and zeros in the z-plane for the circuit shown in Figure. Assume that the operational amplifier is ideal.

This exercise is solved using charge redistribution analysis. The reference directions are shown in Figure 4.1.

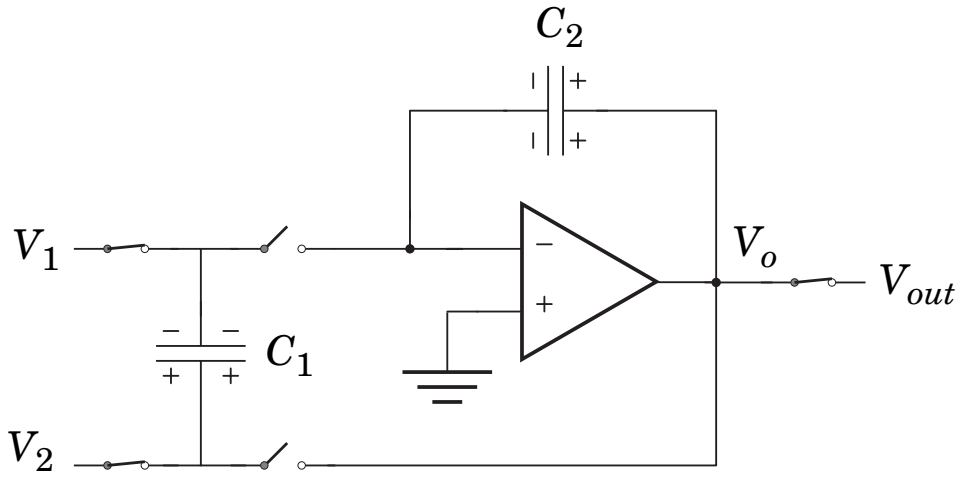

Figure 4.1 The switched-capacitor circuit with reference directions.

First we express the charges over all capacitors at times instances t, $t + \tau$, and $t + 2\tau$.

$q_1(t) = C_1(V_2(t) - V_1(t))$, $q_2(t) = C_2(V_o(t) - 0)$.

At time $t + \tau$

$q_1(t + \tau) = C_1(V_o(t + \tau) - 0)$, $q_2(t + \tau) = C_2(V_o(t + \tau) - 0)$.

At time $t + 2\tau$

$q_1(t + 2\tau) = C_1(V_2(t + 2\tau) - V_1(t + 2\tau))$, $q_2(t + 2\tau) = C_2(V_o(t + 2\tau) - 0)$.

Charge conservation yields

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau) \tag{4.1}$$

and

$$q_2(t+\tau) = q_2(t+2\tau) \tag{4.2}$$

Further we know that $V_{out}(t) = V_{out}(t+\tau) = V_o(t)$.
Eq. (4.2) yields that the output voltage is constant between $t+\tau$ and $t+2\tau$.
Solving the charge conservation yields

$$C_1(V_2(t) - V_1(t)) + C_2V_o(t) = C_1V_o(t+\tau) + C_2V_o(t+\tau) \tag{4.3}$$

which is equal to

$$C_1(V_2(t) - V_1(t)) = (C_1 + C_2)V_o(t+2\tau) - C_2V_o(t). \tag{4.4}$$

Performing z-transformation yields

$$V_o(z)((C_1 + C_2)z - C_2) = C_1(V_2(z) - V_1(z)) \tag{4.5}$$

The output voltage is

$$V_{out}(z) = \frac{C_1}{C_1 + C_2}\frac{V_2(z) - V_1(z)}{z - \frac{C_2}{C_1 + C_2}} \tag{4.6}$$

which is a lossy accumulator, i.e., the pol is located at the positive real axis in the z-plane with a magnitude smaller than one.

b) Is the circuit insensitive of capacitive parasitics. Motivate your answer carefully, $V_{out}(z) = f(V_1(z), V_2(z), V_{os})$.

No, the circuit is not insensitive to capacitive parasitics since the top plate of the capacitor C_1 is charged in the clock phase one and it will be discharged in clock phase two into the sensitive node. The transfer function will be

$$V_{out}(z) = \frac{1}{C_1 + C_2}\frac{C_1V_2(z) - (C_1 + C_p)V_1(z)}{z - \frac{C_2}{C_1 + C_2}}. \tag{4.7}$$

c) The opamp exhibits finite gain, A. Determine the output voltage as a function of the input voltages, $V_{out}(z) = f(V_1(z), V_2(z))$.

The offset voltage is modelled as a voltage source in series with the positive node of the operational amplifier. The finite gain, A, yields that the negative node with the voltage V_x is varying compared to the output node according to

$$V_o = -V_xA \Rightarrow V_x = -V_o/A \tag{4.8}$$

for both clock phases.

The charge redistribution analysis yields

time t:

$$q_1(t) = C_1(V_2(t) - V_1(t)),$$

$$q_2(t) = C_2(V_o(t) - V_{os} - V_x(t)) = C_2\left(V_o(t)\left(1 + \frac{1}{A}\right) - V_{os}\right) \qquad (4.9)$$

time $t + \tau$:

$$q_1(t + \tau) = C_1\left(V_o(t + \tau)\left(1 + \frac{1}{A}\right) - V_{os}\right)$$

$$q_2(t + \tau) = C_2\left(V_o(t + \tau)\left(1 + \frac{1}{A}\right) - V_{os}\right) \qquad (4.10)$$

time $t + 2\tau$:

$$q_1(t + 2\tau) = C_1(V_2(t + 2\tau) - V_1(t + 2\tau))$$

$$q_2(t) = C_2(V_o(t + 2\tau) - V_{os} - V_x(t + 2\tau)) = C_2\left(V_o(t + 2\tau)\left(1 + \frac{1}{A}\right) - V_{os}\right).$$

The charge conservation equations are the same in exercise a).

$$q_1(t) + q_2(t) = q_1(t + \tau) + q_2(t + \tau) \qquad (4.11)$$

and

$$q_2(t + \tau) = q_2(t + 2\tau) \qquad (4.12)$$

Eq. (4.12) yields that the output voltage is constant between $t + \tau$ and $t + 2\tau$. Solving the charge conservation yields

$$C_1(V_1(t) - V_2(t)) + C_2\left(V_o(t)\left(1 + \frac{1}{A}\right) - V_{os}\right) = (C_1 + C_2)\left(V_o(t + 2\tau)\left(1 + \frac{1}{A}\right) - V_{os}\right)$$

The transfer function after the z-transform is

$$V_{out}(z) = \frac{C_1}{(C_1 + C_2)\left(1 + \frac{1}{A}\right)} \frac{V_2(z) - V_1(z) + V_{os}}{z - \frac{C_2}{C_1 + C_2}}. \qquad (4.13)$$

Hence, the gain of the circuit is increase by the finite gain of the opamp. However, in this exercise the opamp does not suffer from offset voltage which yields that

$$V_{out}(z) = \frac{C_1}{(C_1 + C_2)\left(1 + \frac{1}{A}\right)} \frac{V_2(z) - V_1(z)}{z - \frac{C_2}{C_1 + C_2}} \qquad (4.14)$$

5. A mixture of questions

a) Derive the power supply rejection ratio, PSRR, from V_{DD} for the circuit shown in Figure. How can the PSRR be improved by 3 dB?

The small-signal model of the circuit where the power supply voltage is

assumed to be noisy is shown in Figure 5.1.

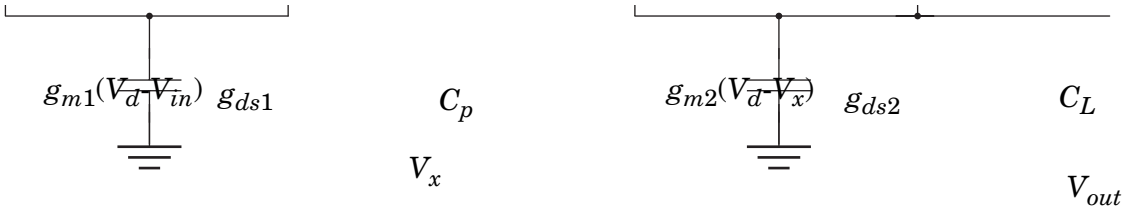

Figure 5.1 The small-signal model of the circuit where V_d is the contribution of the variations at the power supply voltage line.

The PSRR is the ratio between the transfer function from the input to the output compared to the transfer function from the power supply voltage to the output node.

The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1} + sC_p}\frac{g_{m2}}{g_{ds2} + sC_L} \tag{5.1}$$

since V_d is zero. The transfer function from the power supply voltage to the V_x node is given by (assuming the $V_{in} = 0$)

$$\frac{V_x}{V_d} = \frac{g_{m1}}{g_{ds1} + sC_L} \tag{5.2}$$

and the transfer function is than

$$\frac{V_{out}}{V_d} = \frac{g_{m2}}{g_{ds2} + sC_L}\left(1 - \frac{g_{m1}}{g_{ds1} + sC_L}\right) = -\frac{g_{m2}}{g_{ds2} + sC_L}\frac{(g_{m1} - g_{ds1} - sC_L)}{g_{ds1} + sC_L} \tag{5.3}$$

Hence, the power supply voltage is determined as

$$PSRR = \frac{V_{out}}{V_{in}} \Big/ \frac{V_{out}}{V_d} = \frac{g_{m1}g_{m2}}{-g_{m2}(g_{m1} - g_{ds1} - sC_L)} \tag{5.4}$$

Hence, the gain from the input node is smaller than the gain from the power supply voltage to the output node.

b) Why is it important to match the two input transistors in a differential gain stage? Explain three approaches for improving the matching of two transistors.

It is important to have matched transistors in a differential pair in order to both suppress the distortion terms as well as decreasing the offset voltage of the circuit. Matching can be performed in several ways. Increasing the width times the length value is good for matching. Further, lay out the transistors close to each other using the same orientation. Try to decrease the effects of the gradients on the silicon, by utilizing symmetry, for example interdigitized or common centroid layout styles.

c) Determine the minimum output voltage of the circuit shown in Figure. Express it in terms of relevant design parameters.

The minimum output voltage is found by starting at the ground node and finding all paths to the output node. Starting from transistor M_1 yields the

path

$$V_{GS1} + V_{GS2} - V_{GS4} - V_{GS6} + V_{DSAT6}$$
$$= \sqrt{\frac{I_{in}}{\alpha_1}} + V_{TH1} + \sqrt{\frac{I_{in}}{\alpha_2}} + V_{TH2} - \left(\sqrt{\frac{I_{D3}}{\alpha_4}} + V_{TH4} \right) - V_{TH6}. \qquad (5.5)$$

Through the transistor M_3

$$V_{DSAT3} - V_{GS6} + V_{DSAT6} = \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{TH6} \qquad (5.6)$$

while the path from M_5 yields

$$V_{DSAT5} + V_{DSAT6} = \sqrt{\frac{I_{out}}{\alpha_5}} + \sqrt{\frac{I_{out}}{\alpha_6}}. \qquad (5.7)$$

However, which path which is the limiting one depends on the currents in the branches. However, the path through M_3 is not the limiting factor. Hence, the minimum output node voltage is described by

$$V_{out,\,min} = max\left\{ \sqrt{\frac{I_{in}}{\alpha_1}} + V_{TH1} + \sqrt{\frac{I_{in}}{\alpha_2}} + V_{TH2} - \left(\sqrt{\frac{I_{D3}}{\alpha_4}} + V_{TH4} \right) - V_{TH6}, \sqrt{\frac{I_{out}}{\alpha_5}} + \sqrt{\frac{I_{out}}{\alpha_6}} \right\}$$