Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date:	August 14, 2004
Time:	14 – 18
Place:	TER1
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except lap tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Assignments

1. Large-signal analysis

In analog circuit design, it is common to deal with differential amplifiers, either as a single amplifier or as a part of an operational amplifier. In this assignment, a differential amplifier is to be analyzed. Assume that all the transistors are biased in saturation and neglect the body effect. The current through transistor M_5 is I_{bias}.

a) Derive expressions for the common-mode range of the circuit shown in Figure 1.1 as a function of relevant design parameters. (1p)

b) Derive expressions for the output range of the circuit shown in Figure 1.1 as a function of relevant design parameter. Assume that the input common-mode DC voltage is $V_{in,DC} = V_{DD}/2$. (1p)

c) Determine the widths of the transistors $M_1 - M_5$ to obtain $CMR = [CMR_{min}, CMR_{max}]$ and $OR = [OR_{min}, OR_{max}]$ where CMR_{min}, CMR_{max}, OR_{min}, and OR_{max} are given. The lengths of all transistors are L. Note that several solutions exists. (4p)

d) Show that $V_x = V_{out}$ in the operation point ($V_{in,a} = V_{in,b}$) for the circuit in Figure 1.1 given that the transistors M_1, M_2 and M_3, M_4 are perfectly matched. Hint: Assume that $V_{out} > V_x$ and show that it will result in a contradiction. (2p)

e) Compute the output voltage, $V_{out,DC}$, in the operation point ($V_{in,a} = V_{in,b}$) as a function of the bias current and transistor sizes. Neglect the influence of the channel-length modulation. (2p)

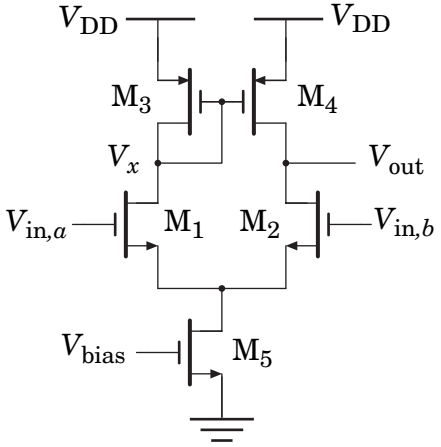

Figure 1.1 Simple amplifiers commonly used as building block in op amps.

2. Small-signal analysis

The transistors in the circuits shown in Figure 2.1a-c are biased in the saturation region and their sizes are equal, i.e., $W_i/L_i = W/L$ for all i. Further, the load capacitances are also equally large and $A \gg 1$. Neglect the influence of all internal parasitics in the transistors.

a) Derive approximate expressions for $g_{m,i}$ and $g_{ds,i}$ for $i = 2, 3, 4, 5$ as a function of $g_{m,1}$ and $g_{ds,1}$, respectively. (2p)

b) Draw the small-signal models of the three amplifiers shown in Figure 2.1 a-c. Do not neglect the influence of the bulk effect. (3p)

c) Compute the small-signal transfer functions, $H(s) = V_{out}(s)/V_{in}(s)$, for the circuits shown in Figure 2.1a-c. Neglect the influence of the bulk effect. (3p)

d) Rank the three stages with respect to the DC gain, first pole, and gain-bandwidth product. (2p)

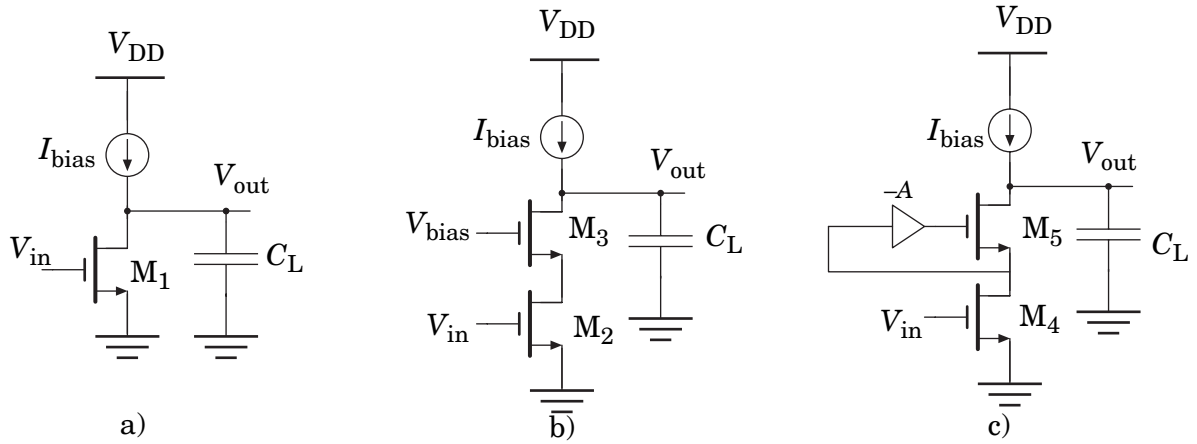

Figure 2.1 Three amplifier structures implemented in CMOS technology.

3. Operational amplifiers

A commonly used building block in analog filtering applications is shown in Figure 3.1.

a) Derive the transfer function from the input of the circuit to its output, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. Assume that all operational amplifiers are ideal. (4p)

b) Consider only the second stage, consisting of resistors R_3 and R_4 and and the operational amplifier. The transfer function from V_x to V_y can be expressed as

$$G(s) = \frac{V_y(s)}{V_x(s)} = K(s)\frac{A(s)}{1 + \beta(s)A(s)} \tag{3.1}$$

where $A(s)$ is the gain of the operational amplifier. Determine expressions for $K(s)$ and $\beta(s)$. (3p)

c) The operational amplifier is implemented as a twostage amplifier and a model for its gain is

$$A(s) = \frac{A_0}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} \tag{3.2}$$

where $|p_1| \ll |p_2|$. Use this model to derive approximate expressions for the unity-gain frequency of the loop gain, $\beta(s)A(s)$, for the second stage in Figure 3.1. (3p)

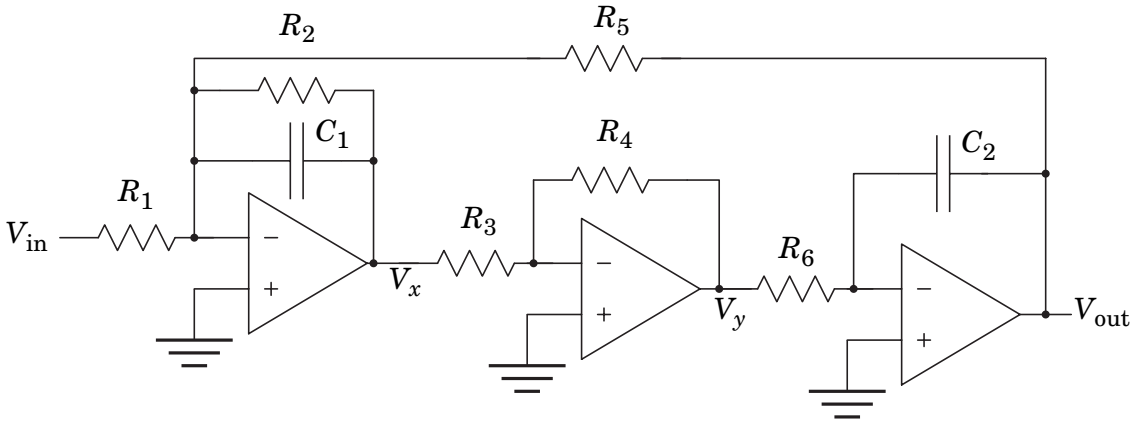

Figure 3.1 Three amplifier analog filtering circuit.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time t, $t + 2\tau$, $t + 4\tau$, etc. is shown in Figure 4.1. Assume that the input signals are constant between clock phase 1 and 2, i.e., $V_1(t) = V_1(t + \tau)$ and $V_2(t) = V_2(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the operational amplifier is ideal. (5p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (1p)

c) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA suffers from an offset voltage, V_{os}. (4p)

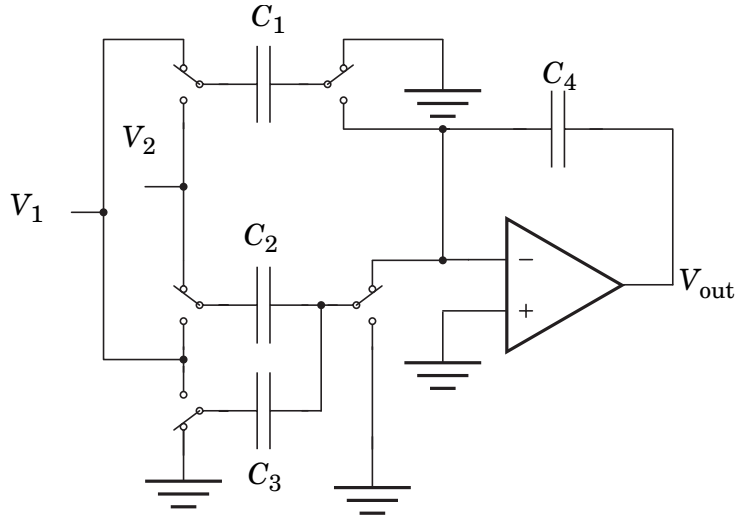

Figure 4.1 A switched-capacitor circuit in clock phase 1.

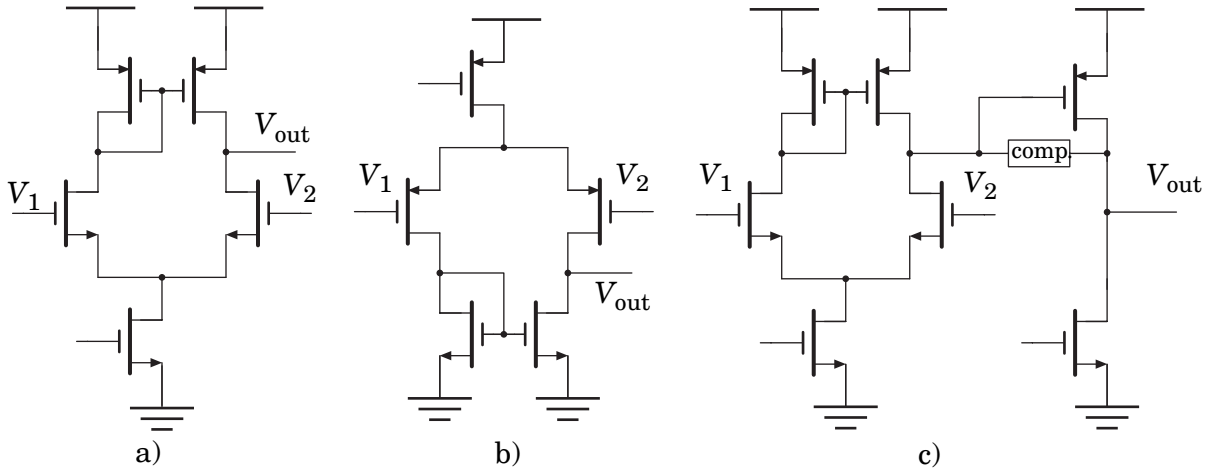

Figure 5.2 Three amplifier stages with positive gain.

5. A mixture of questions

a) Compute the power supply rejection ratio from the positive power supply for the circuit shown in Figure 5.1. (3p)

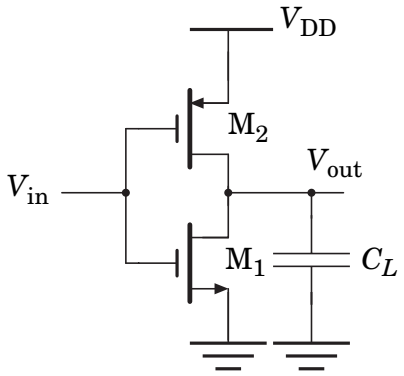

Figure 5.1 An amplifier realized using CMOS transistors.

b) Why do we usually design a common-source amplifier so that the transistors operate in the saturation region? (1p)

c) The amplifier stages shown in Figure 5.2 have positive gain. For each gain stage, determine which terminal, i.e., V_1 or V_2, that is the positive input. (3p)

d) Typically, when designing analog circuits, a bias network is designed to bias all transistors into their desired operation region. A simple biasing network for both NMOS and PMOS current sources are shown in Figure 5.3. Determine the possible interval of the biasing current for which all transistors in the circuit are saturated. Assume that transistors M_1 and M_2 are equally large and neglect the channel-length modulation. (3p)

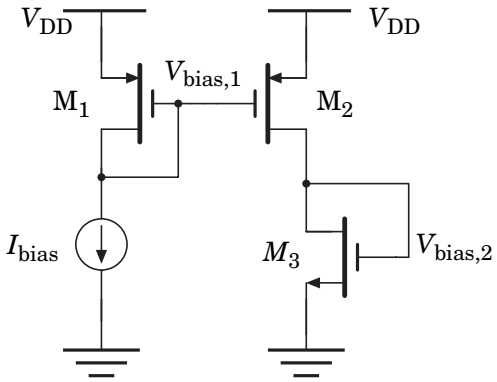

Figure 5.3 A biasing network for NMOS and PMOS current sources.

Transistor formulas and noise

CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

All regions:

$$V_T = V_{T,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$