Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	August 25, 2003
Time:	14 – 18
Max. no of points:	70; 50 from written test, 5 for the project, and 15 for the assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar
Responsible teacher:	Ola Andersson Tel.: 070 - 258 02 95
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Large-signal analysis

The circuit shown in Figure 1.1(a) can be a part of an opamp. In this exercise neglect the channel-length modulation.

a) Determine the output voltage, V_{out}, as a function of the input voltage, V_{in}, for the circuit shown in Figure 1.1(a). Assume that both transistors are saturated. (3p)

b) Determine the DC gain of the circuit by using large-signal analysis. The transistors are operating in the saturation region. (2p)

c) Assume that transistor M_2 is replaced by a resistor, R, as is shown in Figure 1.1(b). Determine the output voltage as a function of the input voltage, $V_{out} = f(V_{in})$. The input voltage ranges from zero to large input voltages, e.g., $V_{in} \gg V_{bias}$. In the graph denote the operation regions of transistor M_1. (5p)

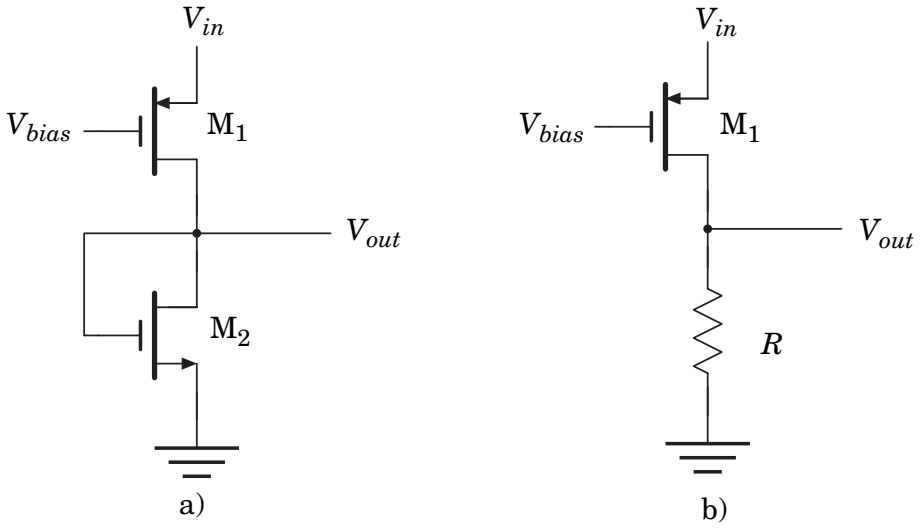

Figure 1.1 A CMOS gain stage.

2. Small-signal analysis

A commonly used circuit in analog design is shown in Figure 2.1. In this exercise assume that all transistors are biased to operate in the saturation region.

a) Derive the transfer function, i.e., V_{out}/V_{in}, of the circuit shown in Figure 2.1(a). Do not neglect the bulk effects. (3p)

b) Derive expressions for the DC gain, first pole, and the unity-gain frequency in terms of I, W, and L for the circuit shown in Figure 2.1(a). Neglect the influence of the bulk effect. (4p)

c) How are the DC gain, first pole, and the unity-gain frequency changed if...
... the current I_1 is increased?
... V_{bias2} is decreased?
... the channel-length of transistor M_3 is doubled?
Assume that the transistors remain saturated. Motivate your answer carefully. (3p)

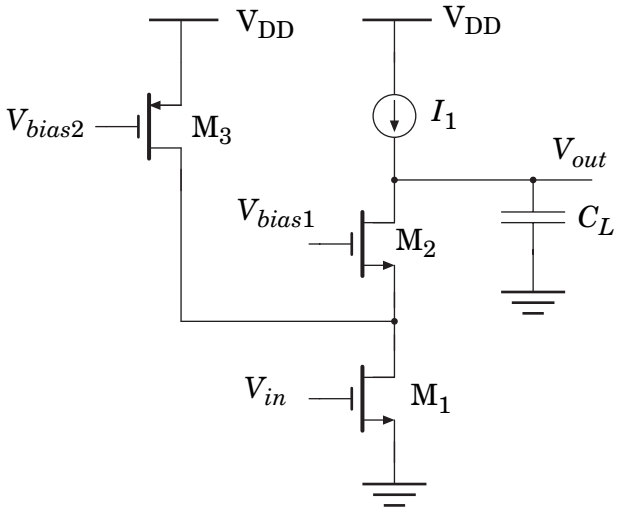

Figure 2.1 A CMOS amplifier structure.

3. Macro block level analysis

The circuit shown in Figure 3.1 is used in all active-RC leapfrog filters.

a) Derive the transfer function from the input to the output, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. Assume that the operational amplifier is ideal except that it suffers from a finite DC gain, i.e., $A(s) = A_0$. Further, what is the minimum DC gain of the opamp in order to have a maximum DC gain error smaller than ε percent for the circuit in Figure 3.1? ε is defined as Eq. (3.1) where H_{ideal} is the transfer function with an ideal opamp while $H_{finitegain}$ is the transfer function with an opamp with finite gain. (6p)

$$\varepsilon = \left| \frac{H_{ideal}(0) - H_{finitegain}(0)}{H_{ideal}(0)} \right| \tag{3.1}$$

b) Assume instead that the amplifier is ideal except that it suffers from an offset voltage, V_{os}. Derive the output voltage as a function of the input and offset voltage. How is the output voltage affected by the offset voltage? (4p)

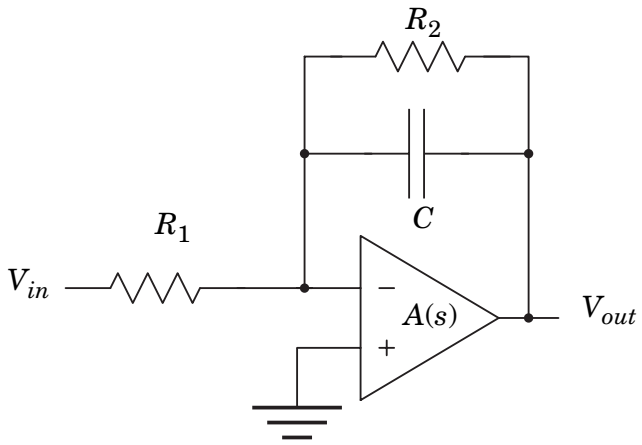

Figure 3.1 The opamp circuit configuration.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure 4.1. The input signal is sampled according to $V_{in}(t) = V_{in}(t + \tau)$.

a) Determine the output voltage as a function of the input voltages, $V_{out}(z) = f(V_1(z), V_2(z))$, and plot the location of the possible poles and zeros in the z-plane for the circuit shown in Figure 4.1. Assume that the operational amplifier is ideal. (4p)

b) Is the circuit insensitive of capacitive parasitics. Motivate your answer carefully. (2p)

c) The opamp exhibits finite gain, A. Determine the output voltage as a function of the input voltages, $V_{out}(z) = f(V_1(z), V_2(z))$. (4p)

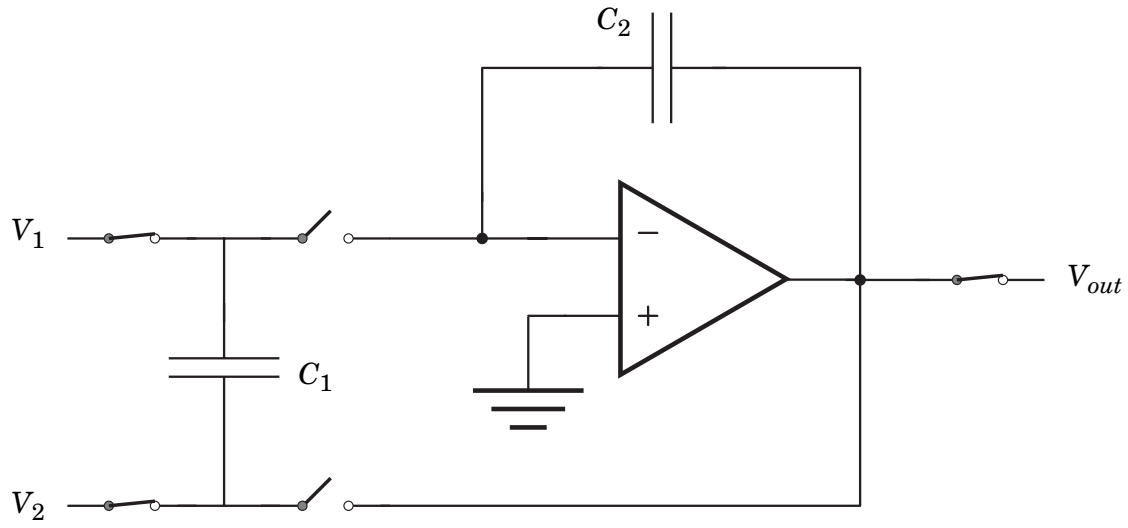

Figure 4.1 A switched-capacitor circuit.

5. A mixture of questions

a) Derive the power supply rejection ratio, PSRR, from V_{DD} for the circuit shown in Figure 5.1. How can the PSRR be improved by 3 dB? (3p)

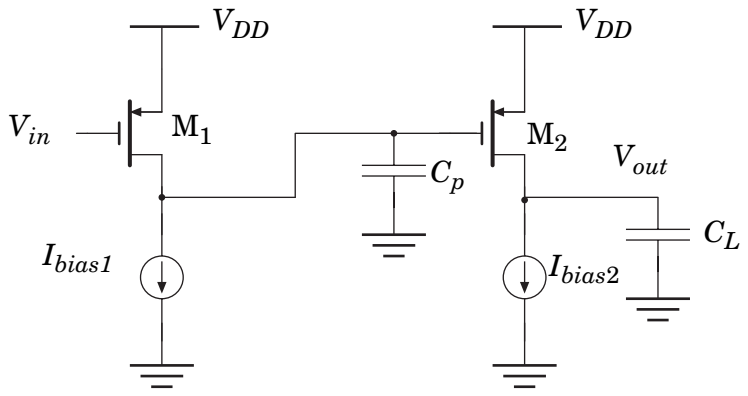

Figure 5.1 A CMOS amplifier structure.

b) Why is it important to match the two input transistors in a differential gain stage? Explain three approaches for improving the matching of two transistors. (4p)

c) Determine the minimum output voltage of the circuit shown in Figure 5.2. Express it in terms of relevant design parameters. (3p)

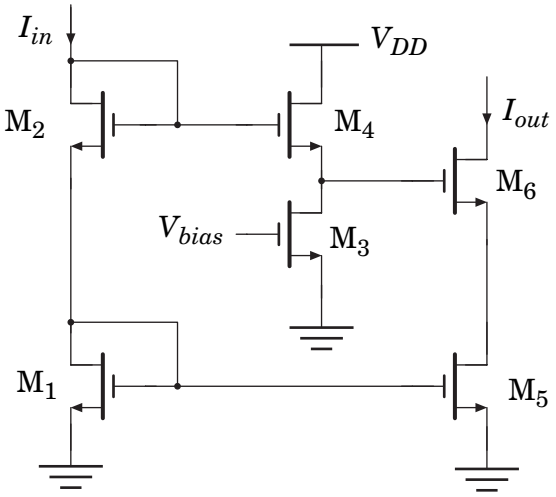

Figure 5.2 A current mirror implemented in CMOS technology.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$