TSEI05, Analog and Discrete-time Integrated Circuits, 20100611
Written exam, TEN1

Date and time	20100611, 14.00 - 18.00
Locations	KÅRA
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	**Any written and printed material, including books and old exams.** **Note! No pocket calculators, no laptops, no ipods, no telephones, no internet connection.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. *x Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **'hidden"in the text** and therefore: read the instructions carefully! *x Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2010-07-01 (hopefully...)

Outline

1. CMOS, PERFORMANCE, ETC. (5 P)

Express the DC gain in terms of V_{bias}, I_D, R_L, and transistor parameters.

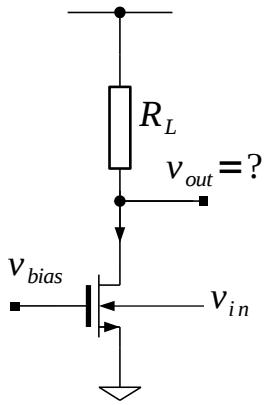

Figure 1.1: Common-something

Draw the small signal schematics and you will get a typical schematic for which you can calculate the DC gain. This small signal schematic will be identical to the standard common-source amplifier. But with the signal connected to bulk rather than gate.

We should therefore use g_{mbs} instead of g_m. This means that the output voltage is given by

$$v_{out}=-v_{in}g_{mbs}/(G_L+g_{ds})\approx -v_{in}g_{mbs}/G_L=-v_{in}g_{mbs}R_L \tag{1.1}$$

The transfer function becomes

$$A_0=\frac{v_{out}}{v_{in}}=\frac{-g_{mbs}}{G_L+g_{ds}}\approx -g_{mbs}R_L \tag{1.2}$$

where we assume that R_L is much smaller than $1/g_{ds}$. We also know that

$$g_{mbs}=\frac{dI_D}{dv_{bs}}=\frac{dI_D}{dv_{eff}}\cdot\frac{dv_{eff}}{dv_{bs}}=g_m\cdot\frac{dv_{eff}}{dv_{bs}}=-g_m\cdot\frac{dv_t}{dv_{bs}}=g_m\cdot\frac{dv_t}{dv_{sb}}=g_m\cdot\frac{0.5\gamma}{\sqrt{V_{SB}+2\phi}} \tag{1.3}$$

We approximate this with $g_{mbs}\approx\eta\cdot g_m$ and the argument is that as long as V_{SB} is not close to -2ϕ (notice the minus), the η is not strongly dependent on V_{SB}. This gives us

$$A_0\approx\frac{-\eta\cdot g_m}{R_L}=\frac{-\eta\cdot\frac{2I_D}{V_{eff}}}{R_L}=\frac{-2\eta\cdot I_D}{(V_{bias}-V_T)\cdot R_L} \tag{1.4}$$

which is a fairly compact expression. Notice that the V_{SB} is part of the V_T in the above expression and one could do some further rewriting to also get the input signal into the expression. One can for example show that

$$g_{mbs}=\frac{0.5\cdot g_m^2\cdot\gamma^2}{g_m\cdot\left(V_{bias}-V_{T0}+\gamma\sqrt{2\phi}\right)-2I_D} \tag{1.5}$$

which gives an expression independent on the v_{sb}. Similar approach can be used to the other expression above.

Express the maximum and minimum input voltage on the bulk terminal.

First of all, the bulk voltage cannot be too high, since we would otherwise open the PN diode. So

$V_{SB}-2\phi>0\Rightarrow 0-v_{in}+2\phi>0\Rightarrow v_{in}<2\phi$ (MOST IMPORTANT ANSWER) (1.6)

Then we also know that the transistor must be conducting which gives us

$$V_{bias}-V_T>0\Rightarrow V_{bias}>V_T\Rightarrow V_{bias}>V_{T0}+\gamma\left(\sqrt{V_{SB}+2\phi}-\sqrt{2\phi}\right) \quad (1.7)$$

which gives

$$\left(\frac{V_{bias}-V_{T0}}{\gamma}+\sqrt{2\phi}\right)^2-2\phi<V_{SB}=0-v_{in}\Rightarrow v_{in}<\left(\frac{V_{bias}-V_{T0}}{\gamma}+\sqrt{2\phi}\right)^2-2\phi \quad (1.8)$$

So just some kind of elaboration on the fact that if V_{bias} and V_T must match.

Further on, we can look at the standard requirement

$$V_{bias}-V_T<V_{ds}=V_{DD}-R_L I_D=V_{DD}-R_L\alpha(V_{bias}-V_T)^2 \quad (1.9)$$

The second-order equation becomes

$$(*)^2+(*)/\alpha R_L-V_{DD}/\alpha R_L=0 \quad (1.10)$$

with solutions

$$(*)=\frac{1}{2\alpha R_L}\pm\sqrt{\frac{1}{(2\alpha R_L)^2}+\frac{V_{DD}}{\alpha R_L}} \quad (1.11)$$

Which gives some indication on how V_{out} and V_{in} must match to guarantee saturation region.

Plot the output DC point as function of the bulk DC point (TSTE08)

So first check what polarity we have (given by the equations above). Increasing V_{IN} decreases the V_{SB}. Decreasing the V_{SB} decreases the V_T. Decreasing the V_T increases the V_{EFF}. Increasing the V_{EFF} increases the current I_D. Increasing the I_D decreases the V_{OUT}. Therefore applying an input signal to the bulk behaves in the same manner as it does for the gate. But there is a nasty square root there. However, still , you do not have to care about that since you only need to sketch.

If one likes, one can go through some rewriting as:

$$I_D = \alpha \cdot \left(V_B - V_{T0} - \gamma \left(\sqrt{V_{SB} + 2\phi} - \sqrt{2\phi} \right) \right)^2$$

$$I_D = \alpha \cdot \left(V_B - V_{T0} + \gamma \sqrt{2\phi} - \gamma \sqrt{2\phi} \sqrt{1 - \frac{v_{in}}{2\phi}} \right)^2 \tag{1.12}$$

$$I_D = \kappa \cdot \left(1 - \psi \sqrt{1 - \frac{v_{in}}{2\phi}} \right)^2$$

etc. But it does not add much value. The idea is to show the square root vs square, etc.

2. GAIN STAGES, SWING, ETC. (5 P)

Derive the 3-dB bandwidth of the circuit as well as the output range for which all transistors are in their saturation regions.

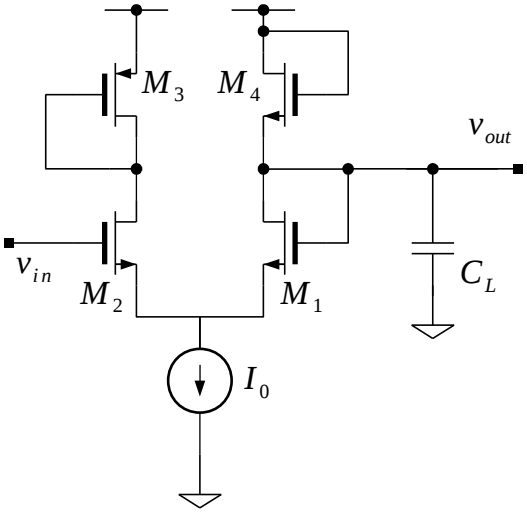

Figure 2.1: Some differential pair of some kind.

First notice that it is a differential gain stage with diode loads, $g_{mP}=g_{m3}$ on one side and $g_{mN}=g_{m4}$ on the other. And then it is coupled in a buffer configuration (gate of M1 connected to output voltage, v_{out}). This means that DC-wise, the gain is unity and the output voltage should track the input voltage.

According to the first order approximation (Yes, you can do this!) the output conductance is essentially given by M4 and M1 in parallel, ie., approximately (two diodes)

$$g_{out}=g_{m1}+g_{m4} \tag{2.1}$$

The 3-dB is then given by the pole, i.e.,

$$p_1=\frac{g_{out}}{C_L}=\frac{g_{m1}+g_{m4}}{C_L} \tag{2.2}$$

We will give correct points for this assumption. It is however not fully correct!

We can take the long and semi-long paths. Look at the small signal schematics including all transistors and assume that the v_c node is not AC grounded. This will gives us a set of three nodes and their corresponding nodal equations become (assuming $g_{mi} \gg g_i$ and grounded input):

(1): $(0-v_x)g_{m3}+(v_c-v_x)g_2+v_c g_{m2}=0$ or $\left((0-v_x)g_{m3}+v_c g_{m2}\approx 0\right)$

(2): $-v_c g_{m2}+(v_x-v_c)g_2+(v_{out}-v_c)g_{m1}=0$ or $\left(-v_c g_{m2}+(v_{out}-v_c)g_{m1}\approx 0\right)$ (2.3)

(3): $(0-v_{out})g_{m4}+i_{out}+(v_c-v_{out})g_{m1}=0$

Notice the fully valid simplistic expression to the right above (within paranthesis) which gives a very fast path to the right answer. The equations can be written as

(1): $v_x(g_{m3}+g_2)=v_c(g_2+g_{m2}) \Rightarrow v_x=v_c\cdot\frac{g_2+g_{m2}}{g_2+g_{m3}}$ or $\left(v_x\approx\frac{g_{m2}}{g_{m3}}\cdot v_c\right)$

(2): $-v_c(g_{m2}+g_2+g_{m1})+v_c\cdot\frac{g_2+g_{m2}}{g_2+g_{m3}}\cdot g_2+v_{out}g_{m1}=0$ or $\left(v_c(g_{m2}+g_{m1})\approx v_{out}g_{m1}\right)$ (2.4)

(3): $-v_{out}(g_{m4}+g_{m1})+i_{out}+v_c\cdot g_{m1}=0$

And further on (to simplify your calculations, you could also assume neglect the g_2 parameter earlier in the calculations as illustrated by the equations in parantheses above).

(4, 1+2): $v_c\cdot((g_{m2}+g_2+g_{m1})(g_2+g_{m3})-(g_2+g_{m2})\cdot g_2)=v_{out}\cdot g_{m1}(g_2+g_{m3})\Rightarrow$

(4): $v_c=v_{out}\cdot\frac{g_{m1}(g_2+g_{m3})}{(g_{m2}+g_2)g_{m3}+g_{m1}(g_2+g_{m3})}$

(5, 3+4): $-v_{out}(g_{m4}+g_{m1})+i_{out}+v_{out}\cdot\frac{g_{m1}^2(g_2+g_{m3})}{(g_{m2}+g_2)g_{m3}+g_{m1}(g_2+g_{m3})}=0$ (2.5)

(5): $-v_{out}(g_{m4}+g_{m1})+i_{out}+v_{out}\cdot\frac{g_{m1}^2}{g_{m2}+g_{m1}}\approx 0\Rightarrow$

(5): $v_{out}(g_{m4}+\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}})=i_{out}$

(Notice that g_{m3} is not part of the expression)

Where (5) in the equation above expresses the output impedance. Assume now that g_{m1} is equal to g_{m2} for symmetry:

$v_{out}(g_{m4}+0.5g_{m1})=i_{out}$ (2.6)

And the output conductance is which in turn gives the output pole and 3-dB frequency.

$g_{out}=g_{m4}+0.5g_{m1}$ (2.7)

so

$p_1=\frac{g_{out}}{C_L}=\frac{0.5g_{m1}+g_{m4}}{C_L}$ (2.8)

Express bandwidth in terms of input DC level (TSTE08)

Since pole is given by

$$p_1 = \frac{g_{out}}{C_L} = \frac{0.5\, g_{m1} + g_{m4}}{C_L} = \frac{\alpha_1 v_{eff,1} + g_{m4}}{C_L} = \frac{\alpha_1 \left(v_{in} - v_c - V_T\right) + g_{m4}}{C_L} \tag{2.9}$$

indicates that the output impedance is linearly dependent on the input DC voltage level.

Maximize bandwidth (TSTE08)

The bandwidth is maximized by maximizing the g_m of the NMOS transistors. So for example increase W and I_D.

Calculating the swing is simple.

The swing is given by the upper range as

$$v_{out} < V_{DD} - V_T - \Delta V \tag{2.10}$$

and lower range as

$$v_{out} > v_{in} - V_T - \Delta V + V_T + \Delta V = v_{in} \tag{2.11}$$

It is an amplifier in a buffer configuration, so the output voltage will track the input voltage. The range for the input voltage is given by

$$V_{DD} - V_T - \Delta V > v_{in} > \Delta V + V_T \tag{2.12}$$

following the same arguments as above which will then give stipulate the range for v_{out}

$$\Delta V + V_T < v_{out} < V_{DD} - V_T - \Delta V \tag{2.13}$$

3. NOISE (5 P)

So, it is a common-gate circuit, with high gain. The output impedance is given by $g_{out} \approx g_3$.

The noise contribution from M3 to output is a standard common source. The output impedance is given by the smaller output resistance from M3. So we have $g_{out} \approx g_3$.

The noise contribution from M1 to output is a standard common source too but with higher gain. The contribution from M2 to output needs a bit of attention. Draw the small-signal schematics.

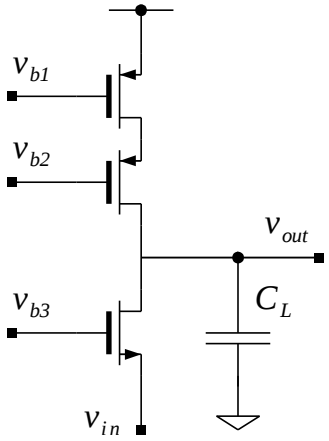

Figure 3.1: Phew! Three transistors...

Total output noise power and the input-referred noise spectral density

Anyway, why not go wild!?!!!?! Set up all the two scaring equations for all those three (gasp!) transistors in one shot and formulate the current laws for the different nodes.

We have only two equations. v_{12} is the intermediate node between M1 and M2.

$$\begin{aligned}&\text{(1):}\quad g_{m1}(0-v_{b1})+g_1(0-v_{12})-g_{m2}(v_{12}-v_{b2})+g_2(v_{out}-v_{12})=0\\&\text{(2):}\quad g_{m2}(v_{12}-v_{b2})+(v_{12}-v_{out})g_2+g_3(v_{in}-v_{out})-g_{m3}(v_{b3}-v_{in})+sC_L(0-v_{out})=0\end{aligned} \tag{3.1}$$

which can be rewritten as

$$\begin{aligned}&\text{(1):}\quad -g_{m1}v_{b1}-v_{12}(g_1+g_{m2}+g_2)+g_{m2}v_{b2}+g_2v_{out}=0\\&\text{(2):}\quad v_{12}(g_{m2}+g_2)-v_{b2}g_{m2}-v_{out}(g_2+g_3+sC_L)+(g_3+g_{m3})v_{in}-g_{m3}v_{b3}=0\end{aligned} \tag{3.2}$$

making the standard assumptions, $g_{ds} \ll g_m$, gives us

$$\begin{aligned}&\text{(1):}\quad v_{12}=\frac{g_{m2}v_{b2}+g_2v_{out}-g_{m1}v_{b1}}{g_1+g_{m2}+g_2}\approx\frac{g_{m2}v_{b2}+g_2v_{out}-g_{m1}v_{b1}}{g_{m2}}\\&\text{(2):}\quad v_{12}g_{m2}-v_{b2}g_{m2}-v_{out}(g_2+g_3+sC_L)+g_{m3}v_{in}-g_{m3}v_{b3}\approx 0\end{aligned} \tag{3.3}$$

Combining the two equations gives us

$$\text{(1+2):}\quad \underbrace{g_{m2}v_{b2}+g_2v_{out}-g_{m1}v_{b1}}_{v_{12}g_{m2}}-v_{b2}g_{m2}-v_{out}(g_2+g_3+sC_L)+g_{m3}v_{in}-g_{m3}v_{b3}\approx 0 \tag{3.4}$$

which becomes

(1+2): $-g_{m1}v_{b1}-v_{out}(g_3+sC_L)+g_{m3}v_{in}-g_{m3}v_{b3}\approx 0$ (3.5)

So, we can write the output as

(1+2): $$v_{out}=\frac{g_{m3}v_{in}-g_{m1}v_{b1}-g_{m3}v_{b3}}{g_3+sC_L}=\frac{\frac{g_{m3}}{g_3}v_{in}-\frac{g_{m1}}{g_3}v_{b1}-\frac{g_{m3}}{g_3}v_{b3}}{1+\frac{s}{g_3/C_L}}$$ (3.6)

Notice now that the M2 is not influencing the result (this is due to the approximation, the M2 is there, but it is much smaller than the other expressions, $g_{m2}+g_2+g_1\neq g_{m2}+g_2$ ...). Anyhow, it can be ignored.

The nice thing is that we have all the sources expressed in one equation. We find the pole to be

$$p_1=g_3/C_L$$ (3.7)

and the DC gain for the different paths are given by

$$A_{0,0}=\frac{g_{m3}}{g_3},\quad A_{0,1}=\frac{-g_{m1}}{g_3},\quad A_{0,3}=\frac{-g_{m3}}{g_3}$$ (3.8)

All noise sources are independent and we can take them one by one using the equation above. Just to wrap up, the output noise spectral density is given by:

$$S_{out}(f)=\left|\frac{g_{m3}/g_3}{1+\frac{s}{g_3/C_L}}\right|^2 S_{in}(f)+\left|\frac{g_{m1}/g_3}{1+\frac{s}{g_3/C_L}}\right|^2 S_1(f)+\left|\frac{g_{m3}/g_3}{1+\frac{s}{g_3/C_L}}\right|^2 S_3(f)$$ (3.9)

We can also directly apply the brickwall concept and multiply the DC gain with the $p_1/4$ to find the total noise power. Further on, from a noise point of view, the input is grounded, so

$$P_{out}=A_{0,1}^2\cdot\frac{p_1}{4}\cdot\frac{4kT\gamma}{g_{m1}}+A_{0,3}^2\cdot\frac{p_1}{4}\cdot\frac{4kT\gamma}{g_{m3}}=\frac{g_{m1}^2}{g_3^2}\cdot\frac{g_3}{4C_L}\cdot\frac{4kT\gamma}{g_{m1}}+\frac{g_{m3}^2}{g_3^2}\cdot\frac{g_3}{4C_L}\cdot\frac{4kT\gamma}{g_{m3}}$$ (3.10)

$$P_{out}=\frac{g_{m1}}{g_3}\cdot\frac{1}{C_L}\cdot\frac{kT\gamma}{1}+\frac{g_{m3}}{g_3}\cdot\frac{1}{C_L}\cdot\frac{kT\gamma}{1}=(g_{m1}+g_{m3})\frac{kT\gamma}{g_3C_L}$$

Input referred noise spectral density

To calculate the input-referred noise spectral density, we take the output noise density and divide with the transfer function from input to output. This gives us

$$S_{in}(f)=\frac{\left|\frac{g_{m1}/g_3}{1+\frac{s}{g_3/C_L}}\right|^2 S_1(f)+\left|\frac{g_{m3}/g_3}{1+\frac{s}{g_3/C_L}}\right|^2 S_3(f)}{\left|\frac{g_{m3}/g_3}{1+\frac{s}{g_3/C_L}}\right|^2}=\frac{g_{m1}^2}{g_{m3}^2}\cdot S_1(f)+S_3(f) \tag{3.11}$$

Which can be written as

$$S_{in}(f)=\frac{g_{m1}^2}{g_{m3}^2}\cdot\frac{4kT\gamma}{g_{m1}}+\frac{4kT\gamma}{g_{m3}}=4kT\gamma\cdot\frac{g_{m1}}{g_{m3}}\cdot\left(1+\frac{1}{g_{m3}}\right) \tag{3.12}$$

The input-referred noise depends on the width of M3 (TSTE08)

The current through the circuit is set by the PMOS transistors and is not a design parameter with respect to transistor M3. We can then for example use

$$g_{m3}=2\sqrt{\kappa W_3 I_D}=\psi\sqrt{W_3} \tag{3.13}$$

and we have

$$S_{in}(f)\sim\frac{A}{\sqrt{W_3}}+\frac{B}{W_3} \tag{3.14}$$

which can be used to sketch the relationship. Small W high noise, large W low noise.

4. OP/OTA (5 P)

Express two shortcomings

Start with setting up what we know: The transfer functions in open loop and closed loop. The open loop transfer function looks like:

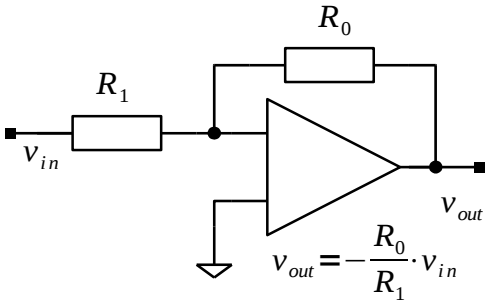

Figure 4.1: Closed-loop gain configuration.

$$v_{OP,out}(s)=v_{OP,in}(s)\cdot\frac{A_0}{1+s/p_1} \tag{4.1}$$

so we can set up the relations for the closed-loop amplifier

$$\begin{aligned}&(1):\quad \left(v_{in}+v_{OP,in}\right)\cdot G_1+\left(v_{out}+v_{OP,in}\right)\cdot G_2=0\Rightarrow v_{in}G_1+v_{out}G_2=-v_{OP,in}\left(G_1+G_2\right)\\ &(2):\quad v_{OP,out}=v_{out}=v_{OP,in}\cdot\frac{A_0}{1+s/p_1}\end{aligned} \tag{4.2}$$

Combining the two gives

$$(1+2):\quad -v_{out}=\frac{A_0}{1+s/p_1}\cdot\frac{v_{in}G_1+v_{out}G_2}{G_1+G_2}$$

$$\Rightarrow v_{out}\left(1+\frac{A_0}{1+s/p_1}\cdot\frac{G_2}{G_1+G_2}\right)=\frac{-A_0}{1+s/p_1}\cdot\frac{G_1}{G_1+G_2}\cdot v_{in} \tag{4.3}$$

$$\frac{v_{out}}{v_{in}}=\frac{-A_0\cdot G_1}{\left(1+s/p_1\right)\cdot\left(G_1+G_2\right)+A_0\cdot G_2}=-\frac{G_1}{G_2}\cdot\frac{1}{1+\frac{G_1+G_2}{A_0G_2}+s\cdot\frac{G_1+G_2}{p_1A_0G_2}}$$

We will rewrite this slightly as

$$\frac{v_{out}}{v_{in}}=-\frac{G_1}{G_2}\cdot\frac{1+\frac{G_1+G_2}{A_0G_2}}{1+s\cdot\frac{G_1+G_2}{p_1A_0G_2\left(1+\frac{G_1+G_2}{A_0G_2}\right)}}=-\frac{G_1}{G_2}\cdot\frac{1+\frac{G_1+G_2}{A_0G_2}}{1+\frac{s}{p_1\cdot\left(\frac{A_0G_2}{G_1+G_2}+1\right)}} \tag{4.4}$$

Now we can see the two short comings in the equation above:

One DC error

$$\Delta A_{CL} = 1 + \frac{G_1 + G_2}{A_0 G_2} = 1 + \frac{R_2/R_1 + 1}{A_0} \tag{4.5}$$

and a limited bandwidth of

$$p_x = p_1 \cdot \left(\frac{A_0 G_2}{G_1 + G_2} + 1 \right) = p_1 \cdot \left(\frac{A_0}{R_2/R_1 + 1} + 1 \right) \tag{4.6}$$

So answers could be:

- The limited DC open-loop gain introduces a DC gain error in the closed loop.
- The limited DC open-loop gain affects the closed-loop bandwidth.
- The limited pole affects only the closed-loop bandwidth.
- If the gain, A_0, is very, very high, the limited pole plays less of a role.
- If the closed loop gain is very high, the errors will become more dominant (!). With high close-loop gain we are mimicking the open-loop behavior.

Derive how the swing is affected by limited current (TSTE08)

The maximum output current delivered by the opamp is I_0. This means that a maximum of I_0 can flow through the R_0 resistor (referred to as R_2 in the solutions above). According to Mr. Ohm, the maximum voltage across the resistor will then be $V_0 = R_0 I_0$. Further we assume that the high DC gain, A_0, is maintained during the proper range, which also indicates that the maximum output voltage that can be delivered is

$$v_{out,max} = V_0 \cdot (1 - 1/A_0) \approx V_0 \Rightarrow v_{out,max} = R_0 I_0 \tag{4.7}$$

A graph could show this quite elegantly.

5. DATA CONV'S, NOISE, ETC. (TSEI05) (5 P)

When is the peak output thermal noise current density less than the quantization noise power density

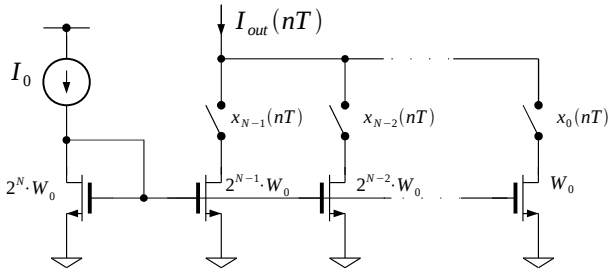

Figure 5.1: Current-steering D/A converter

For this current-steering data converter all currents are directed to the output. The same must hold for all the noise. For the peak noise, all switches are conducting and all noise/current go to the output. Due to the current mirror and all connected gates together, the V_{eff} must be constant and same for all sources. This makes it practical to use

$$g_{m,k} = \frac{2I_{D,k}}{V_{eff}} = \frac{2 \cdot 2^k \cdot \frac{I_0}{2^N}}{V_{eff}} = \frac{I_0}{V_{eff} \cdot 2^{N-1}} \cdot 2^k \tag{5.1}$$

to express the transconductance for the k th source. Notice, as for now, the W_0 is not part of the expression. If we for the time being neglect the bias source, the total peak noise current at the output must be given by the sum of all current sources including the bias source:

$$S_{i,tot}(f) = S_{i,0}(f) + S_{i,1}(f) + \ldots + S_{i,N-1}(f) + \underbrace{\frac{(2^N-1)^2}{2^{2N}} \cdot S_{i,N}(f)}_{\text{bias}} \tag{5.2}$$

notice the weighting of the bias source to output, which is approximately unity. This means we have the total noise power as

$$S_{i,tot}(f) = \sum_{k=0}^{N} S_{i,k}(f) \tag{5.3}$$

Inserting the expression on $g_{m,k}$ and the spectral density $S_{i,k}(f) = 4kT\gamma g_{m,k}$, we get:

$$S_{i,tot}(f) = 4kT\gamma \sum_{k=0}^{N} g_{m,k} = \frac{kT\gamma I_0}{V_{eff} \cdot 2^{N-3}} \cdot \sum_{k=0}^{N} 2^k = \frac{kT\gamma I_0}{V_{eff} \cdot 2^{N-3}} \cdot \frac{2^{N+1}-1}{2-1} \tag{5.4}$$

We now sum that the number of bits is fairly large and we can approximate:

$$S_{i,tot}(f) \approx \frac{kT\gamma I_0}{V_{eff}} \cdot 2^4 \tag{5.5}$$

We see from the bias source that

$$I_0 = \alpha_N \cdot V_{eff}^2 = \kappa\, 2^N W_0 V_{eff}^2 \Rightarrow V_{eff} = \sqrt{\frac{I_0/\kappa}{2^N W_0}} \tag{5.6}$$

We use this to eliminate the V_{eff} in the expression above:

$$S_{i,tot}(f) \approx k\,T\,\gamma\,\sqrt{\kappa I_0}\cdot\sqrt{W_0}\cdot 2^{4+N/2} \tag{5.7}$$

So now, let's look at the quantization noise. Within the Nyquist range, the total noise power is given by:

$$Q_{tot} = \frac{\Delta^2}{12} = \frac{(I_0/2^N)^2}{12} \tag{5.8}$$

The total thermal noise in the Nyquist range is given by

$$P_{tot} = f_s \cdot S_{i,tot}(f) = f_s \cdot k\,T\,\gamma\,\sqrt{\kappa I_0}\cdot\sqrt{W_0}\cdot 2^{4+N/2} \tag{5.9}$$

So for $P_{tot} = Q_{tot}$ we have

$$\frac{I_0^2}{3\cdot 2^{2N+2}} = f_s \cdot k\,T\,\gamma\,\sqrt{\kappa I_0}\cdot\sqrt{W_0}\cdot 2^{4+N/2} \Rightarrow$$

$$W_0 = \left(\frac{I_0^{3/2}}{3 f_s \cdot k\,T\,\gamma\,\sqrt{\kappa}\cdot 2^{6+5N/2}}\right)^2 \sim \frac{\Phi}{2^{5N}} \tag{5.10}$$

6. SC CIRCUITS (TSTE08) (5 P)

Derive the transfer function from input to output

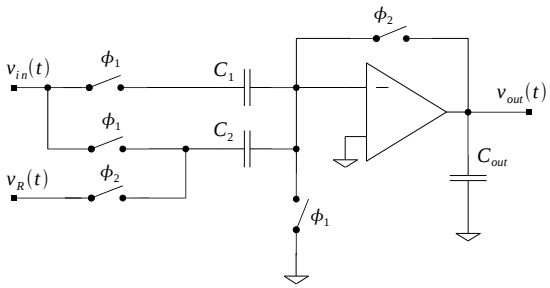

Figure 6.1: An SC circuit.

We have two input signals and one output signal. Set up the charge distribution and charge preservation for the two phases.

For the first phase we have:

$$q_1(n)=C_1\left(v_1(n)-0\right)=C_1\cdot v_1(n)$$
$$q_2(n)=C_2\left(v_1(n)-0\right)=C_2\cdot v_1(n) \quad (6.1)$$

Further on, we see that the negative input of the OTA is connected to ground, which means that the charge input voltage is (ideally) 0 which also forces the output to be 0, i.e.,

$$v_2(n)=0 \quad (6.2)$$

For the second phase we get

$$q_1(m)=C_1\left(v_x(m)-v_{out}(m)\right)$$
$$q_2(m)=C_2\left(v_2(m)-v_{out}(m)\right) \quad (6.3)$$

Notice the disconnected plate of C_1 and we must have a floating node. Further on, we see that the positive input of the OTA is connected to ground, and the OTA is connected in a buffer configuration which means that the output voltage is (ideally) 0 which also forces the output to be 0, i.e.,

$$v_2(m)=0 \quad (6.4)$$

The output is always zero. During phase 2, the C_2 is recharged, but only between the ideal amplifier and the ideal input voltage source.

Explain if the circuit is sensitive to parasitics or not.

No

What kind of circuit is this?

It is something strange with the circuit and C_1 and C_2 do not influence the result.