# TSEI05, Analog and Discrete-time Integrated Circuits, 20100611
# Written exam, TEN1

| | |
|---|---|
| **Date and time** | 20100611, 14.00 - 18.00 |
| **Locations** | KÅRA |
| **Responsible teacher** | J Jacob Wikner, jacwi50, +46-70-5915938 |
| **Aid** | **Any written and printed material, including books and old exams.**<br>**Note! No pocket calculators, no laptops, no ipods, no telephones, no internet connection.** |
| **Instructions** | A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five.<br>✗ *Hint!* ***Be strategic*** *when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...*<br>Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text).<br>Also note that the questions in this exam are divided into logical sections.<br>You may use **Swedish, English or German** in your answers.<br>Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully!<br>✗ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.* |
| **Results** | Available by 2010-07-01 (hopefully...) |

**Outline**

# 1. CMOS, PERFORMANCE, ETC. (5 P)

Consider the circuit in the figure below. Assume that the signal is fed through the bulk of the NMOS transistor rather than the gate. Further, assume that the transistor behaves according to the "school book", i.e., for saturation region we have

$$I_D=\alpha\cdot\left(V_{GS}-V_T\right)^2 \text{ where } \alpha=\frac{\mu_0 C_{ox}}{2}\cdot\frac{W}{L}. \quad (1.1)$$

and for the threshold voltage we have

$$V_T=V_{T0}+\gamma\cdot\left(\sqrt{V_{SB}+2\phi}-\sqrt{2\phi}\right) \text{ where } V_{T0},\ \gamma, \text{ and } \phi \text{ are parameters.} \quad (1.2)$$

Let's derivate! So, the signal is - as you can see in the figure - applied to the bulk rather than any of the other fun terminals.

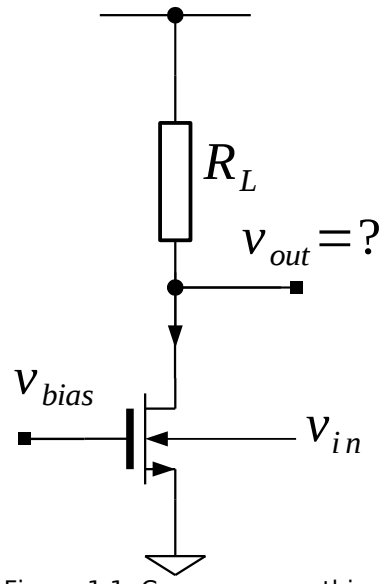


Figure 1.1: Common-something

**Express the DC gain in terms of $V_{bias}$, $I_D$, $R_L$, and transistor parameters.** Minimize the degree of freedom in your expression. Make reasonable assumptions (and motivate them). Since you will find some of these results in your notes, we want to see some good derivations in your answers...

Then express **the maximum and minimum input voltage on the bulk terminal**, such that the transistor is still in its saturation region. You probably need to use the $V_{bias}$ and $V_{out}$ voltage in your expression.

- *This exercise will show that you have understood basic small-signal properties. It always helps with some figures for the small signal schematics too.*
- *Hint: How negative can the bulk terminal be? And also, do not forget the sign.*

# 2. GAIN STAGES, SWING, ETC. (5 P)

Consider the circuit in Figure 2.1 which is some kind of differential pair or so. You have two things to do for this exercise:

**Derive the 3-dB bandwidth** of the circuit as well as the **output range** for which all transistors are in their saturation regions.

Make valid assumptions and motivate them well in your solutions.

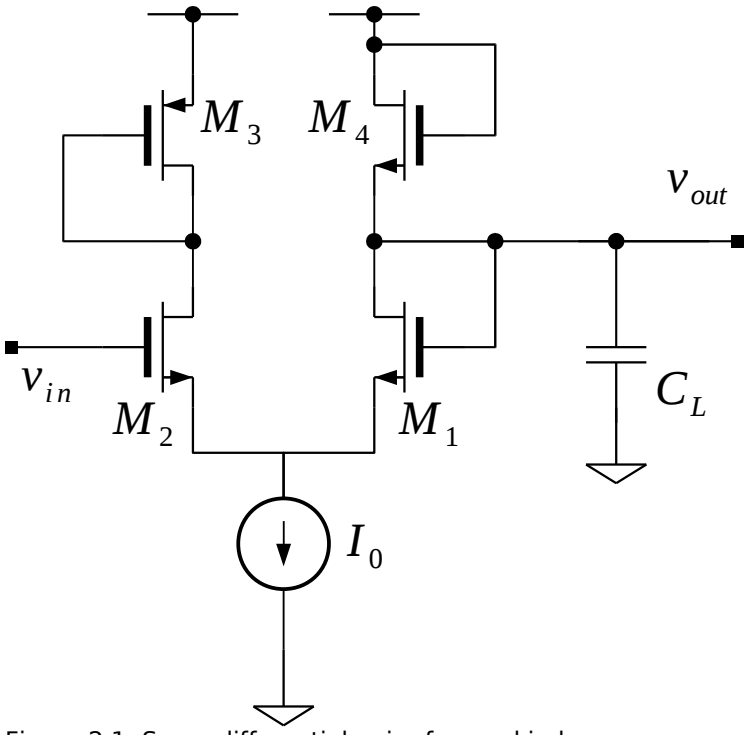


Figure 2.1: Some differential pair of some kind.

- *This exercise will show that you have understood the relation between schematics and small-signal expressions as well as large-signal operation.*
- *Don't forget to sanity check your results! Hint: what should the DC gain be?*

# 3. NOISE (5 P)

Consider the circuit in Figure 3.1 which consists of two PMOS and one NMOS transistor. With your experience you see that it is a common-gate stage. All transistors operate in their saturation regions.

Assume that all transistors are noisy and derive the **total output noise power and the input-referred noise spectral density** of the circuit.

Once again, this is a rather standard exercise for which you will find answers in the books and your notes. Therefore, we **require clear illustrative solutions**.

Also, express **how the input-referred noise depends on the width** of the transistor connected to $V_{b3}$. Sketch a diagramme showing the spectral density as function of $W_3$.

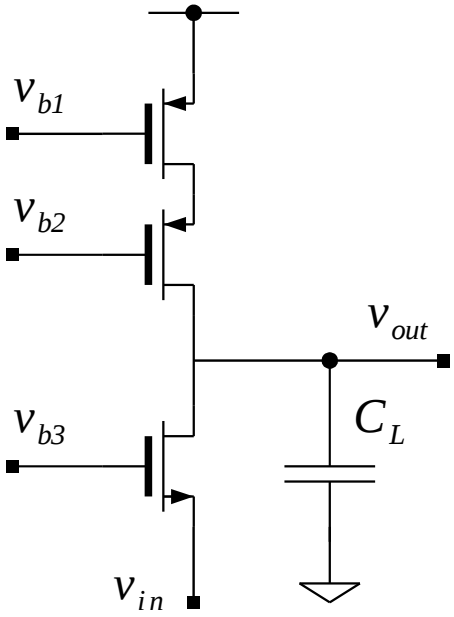

Figure 3.1: Phew! Three transistors...

- *Tip 1: Parts of this exercise is found in the course exercises!*
- *Tip 2: Use all the symmetries to speed up your conclusions.*
- *Tip 3: To find max SNR, minimize the expression w.r.t. the number of parameters.*
- *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth: $p_1/4$ (see for exampleJohns Martin).*

# 4. OP/OTA (5 P)

OK, so a question about OP/OTA. Consider the feedback configuration in Figure 4.1. Now, assume the following transfer characteristics for the **open-loop amplifier**:

$$v_{OP,out}(s)=v_{OP,in}(s)\cdot\frac{A_0}{1+s/p_1}$$ where $A_0$ is a finite constant. (4.1)

Assume that the $p_1$ pole does not shift its position when the OP/OTA is in a feedback configuration. (This means that the $p_1$ pole is set internally in the OP/OTA and independent on the load).

**Derive the overall transfer function** for the amplifier and **express two shortcomings** compared to an ideal amplifier that this configuration suffers from, i.e., compare your results with the ideal transfer function:

$$v_{out}(s)=-\frac{R_0}{R_1}\cdot v_{in}$$ (4.2)

*✗ For maximum number of points: don't just answer "property X is different". Isolate this property in your expression, motivate how and what impact it has on the overall transfer function!*

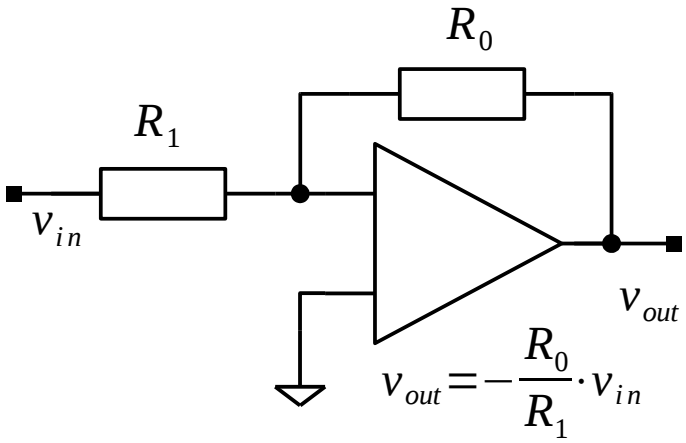


Figure 4.1: Closed-loop gain configuration.

*✗ Once again! Any (reasonable) try to answer the question can give you*

*credits!*

# 5. DATA CONVERTERS AND NOISE, ETC. (5 P)

Whew! Finally... the last question (this time...) Let's spend that on data converters (and noise again...).

Assume that you have an $N$-bit D/A converter producing an output current between 0 and (approximately) $I_0$ A. For a standard, current-steering D/A converter, the analog output current (at a certain multiple of the sampling period) is given by

$$i_{out}(nT)=\left(x_0(nT)+x_1(nT)\cdot 2+x_2(nT)\cdot 2^2+\ldots+x_{N-1}(nT)\cdot 2^{N-1}\right)\cdot\frac{I_0}{2^N} \tag{5.1}$$

where $x_i(nT)$ are the digital control bits. This converter is illustrated by Figure 5.1.

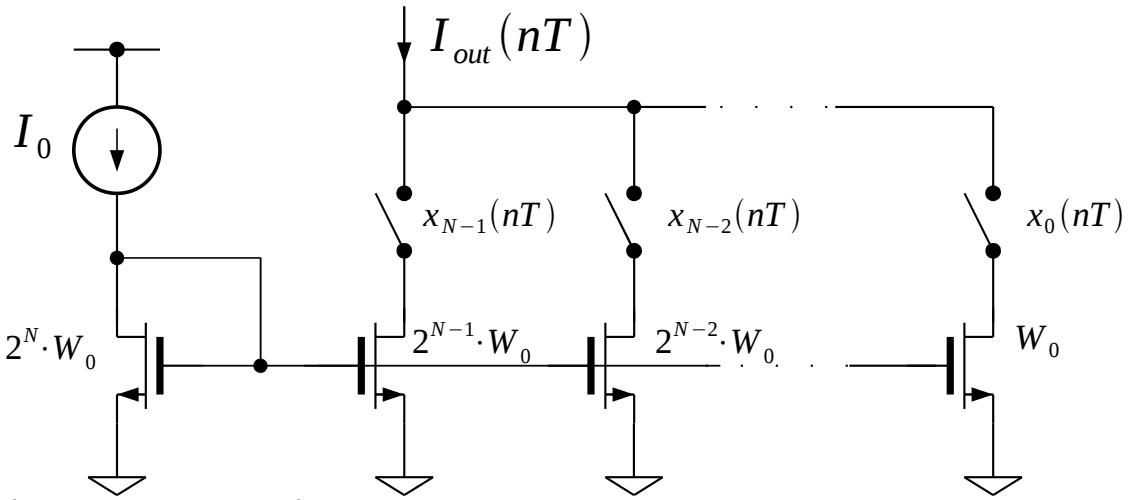


Figure 5.1: Current-steering D/A converter

Your mission is now to determine for which transistor widths, $W_0$, the **peak output thermal noise current density is less than the quantization noise power density**. $I_0$, $T$, and $N$ are fixed design parameters.

Assume that all transistors are noisy, but limit the answer to thermal noise current $(4kT\gamma g_m)$.

- *Tip 1: The exercise is not as difficult as it first appears to be!*
- *Tip 2: Look at currents only. For peak current -- all switches are conducting to the output.*
- *Hint 1: Remember how we elaborated on quantization noise spectral density in e.g. oversampling/interpolating data converters and how the sample frequency plays a role!*

*✗ Tip 3: Don't forget the noise of the bias transistor.*