Lesson 6

7.1) The indicated waveforms are applied to the JK master-slave flip-flop of Fig 7.1. For this problem, assume that gate delays are short compared to the input signal time scale.

a) Sketch the waveforms that appear at the Q_M and Q_S outputs of the master and slave latches. Assume that the flip-flop is initially in the reset state.

b) Do the waveforms exhibit any 1's catching behavior?

Figure 7.1. JK master-slave flip-flop.

7.2) Consider dynamic implementations of the D flip-flop using either the C^2MOS approach of Figure 7-26 or the TSPC approach of Figure 7-33. The flip-flops are driven by clocks CLK and CLK with a 50% duty cycle.

a) Discuss the impact of clock overlap on the behavior of both flip-flops.

b) Discuss the impact of finite clock rise and fall times on the behavior of both flip-flops.

7.3) Design a pipelined circuit of the function F = (AB+BC)+D. Use C^2MOS latches for the implementation.

a) Draw the schematics of the circuit assuming you are allowed to introduce two pipeline stages between input and output. Try both static and dynamic implementations of the logic. Place the latches so that a maximum clock speed is obtained. What limits clock speed in both cases?

Stefan Andersson, Erik Backenius, Peter Caputa, Timmy Sundström

7.4) A five-stage ring oscillator is selected for the implementation of a VCO. The oscillation frequency should be 5MHz for a supply voltage of 3.3V. The basic inverter circuit used in the oscillator is shown in Fig. 7.2. Due to their large sizes, you may consider transistors M2 and M3 to be ideal switches (with zero on-resistance).

a) Determine the DC-voltages needed at nodes H and L to get the required oscillation frequency. Consider only the capacitance shown in the figure. Ignore the channel length modulation factor. Also make sure that rise and fall times are identical. Use the following transistor parameters:

 k_n '=19.6 μ A/V², k_p '=5.4 μ A/V², V_{tn} =0.743 V, V_{tp} =-0.739 V L=0.9 μ m, W_1 =5 μ m, W_2 =100 μ m, W_3 =300 μ m, W_2 =10 μ m

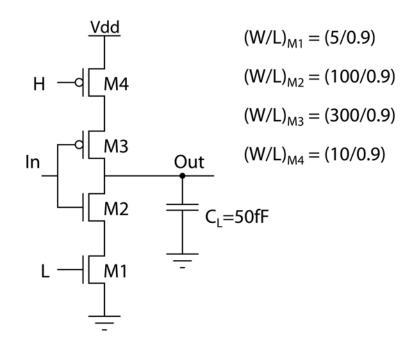


Figure 7.2. Current-starved inverter used in the oscillator.

7.5) Design a finite state machine with the use of registers, multiplexers, inverters, AND-gates and OR-gates, fulfilling the graph shown in Figure 7-3.

Data inputs: *a*, *b*, *c* Data output: *y*

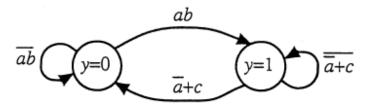


Figure 7-3. A finite state machine

7.6) Design a finite state machine with the use of registers, multiplexers, inverters, ANDgates and OR-gates, fulfilling the graph shown in Figure . Data inputs: a, b, c Data output: y (y0y1)

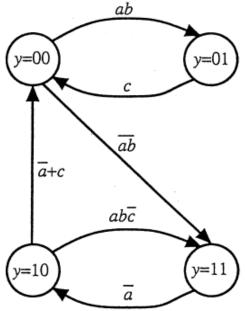


Figure 7-4. A finite state machine



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	Do, the wave form YES, the J=1 gli Que is set even the the p-cycle. Hint! IK-flip flop	s exhibit ony 1.5 c itch is caught: high I rehrus to zero	to the given figure and see what happens at nodes Qm, an Qs, Qs atching behavior?

Consider dynamic implementations of the Difilip-flop Using either the comos approach of figure 7-26 or the TSPC approach of 7-33. The flip flops are driven by clocks of and of with a 50% y cy de Vad -15 17 1 Įø ø ø ය In D D ø 1 1 Positive edge-triggered Di flip-flip (flig-7-33) + + + + + + + + + q2 mos master-slave Diflip-flop (Fig 7-26) 1Chig (impact pt dock overlap behavior of both Discuss the the or Hip-Hops Fig 7-26 分 f o d (1-1) overlap (0-0) onoriap • A race thyough the diversities not possible since rage Hhruugh the circuit A is not possible since only PUN- networks are active PDny-networks are active ļ Fig 7-33 achivated, but never Pyn or Ppn Rafe is not possible only are Simultaneous timite clock I rise and fall times b) Discuss the impact of on the behavior of both flip-flops! For sufficiently slow rise fall times, bothi n- and p-channel devices can confutti signal toingously, Race 15 possible.

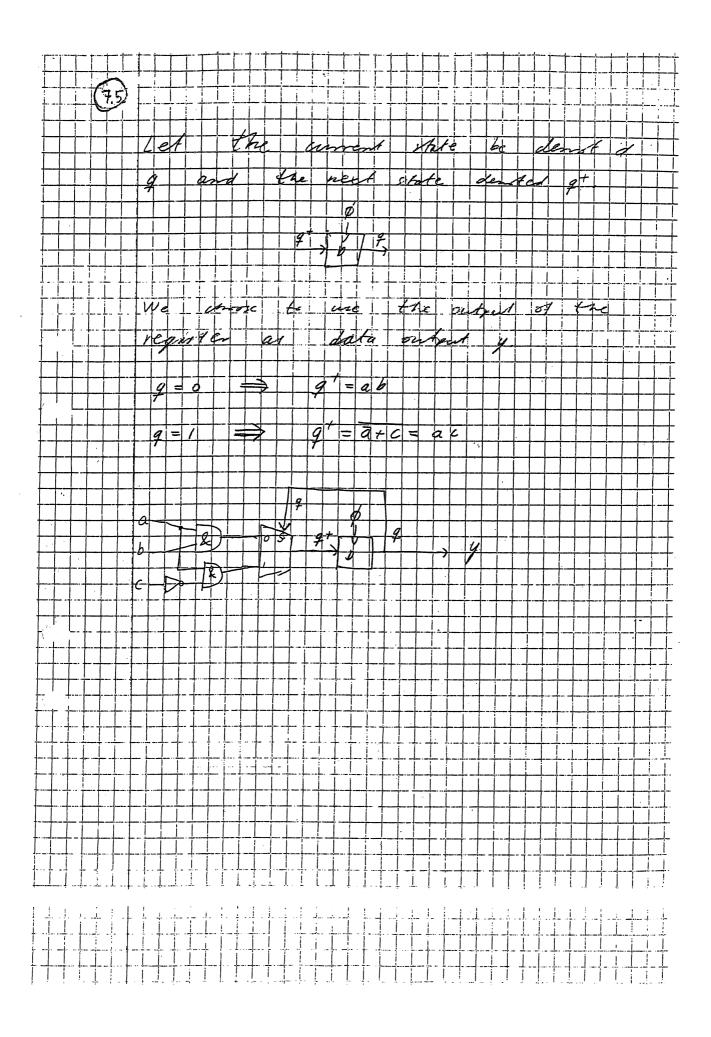
Design a pipelined circuit of the function F=(AB+BC)+D. Use C²MOS-latches for the implementation. a) Draw the schematics of the circuit assuming you are allowed to introduce two pipeline stages between inpit and output. Try both static and dynamic implementations of the logic. Place the latches so that a maximum clock speed is dottained. What Itmits clock speed in both cases ? C2MOS latcher INVERT data; rearrange the function to preficine for the $F = AB + BC + D = \overline{AB} \cdot \overline{BC} \cdot \overline{D}$ P DYNAMICT IMPLEMENTATION AB BÎ l₿⇒ evalis np-call & ø-latch Ø-latch PARTIAL CIRCUITRY 18-dE ø. Ø J-B AB Ø 11 i P. logic Ø-laitch N-llogic Eval Evol Ø ynamic NAND dynamic INV four is limited by Sinput Nor and delay through a register. ÷ 1

IMPLEMENTATION ; 73 STATIC To avoid race, only non-inverting logic can be placed between registers. Up to the second pipeline, register are the same However: continued ... registers ÷ 1 -----AB static ļ latch i Ì stati Must have a static on the output gale 1 1 Ì I Ø-latch 1 1 by į I 3-input Nor, inverter tedi Irequisteri. and 1 ļ . Ī 1 l j l J J 1 1 ľ ì 1 ! I 1 i ļ l j i i 2 J : I l i Ï í 1 ï 1 į j i i 1 j 1 Ì 1 Į 1 ĺ İ Í ļ 1 i Ì ł ł • 1 i ÷ ł ł ł : I ł į 1 1 ł ł 1 i ÷ ! ļ ļ i į 1 i ÷ į i İ į i ł ļ ÷ 1 ; ÷ 1 ! ÷ ļ l ı ł ! ļ ! į į ļ į I i 1 ł i i ł I ì ł ī İ.

A five-stage ring oscillator is selected for Me implementation of a vco. The oscillation frequency should SMHZ for a be : supply voltage of 3,3V. The circuit used in the basic invover osciillator is shown in figure 6.61. Due to their large ¿izes and МЗ consider transistors M12 i tạ be You may (with pero on-resistance) switches $(W/F)_{M1} = (5/1,2)$ $(W/F)_{M2} = (100/7,2)$ H-01 MH (100/1.2) (W/L) M3 = (300/1.2) CL = SOFF L . 715 MI (WIL) my = (10/12) a) Determine the DO-voltages needed at nodes it and 1 to get the required oscillation frequency. Consider Duly the capacitu in the figure. Ignore the channel length modulation pictor. Also make sure the mise and fall times are equal. For a ring oscillator we have the oscillation period T = 2 tp. N R = 2 tp. N

 $T = 2 tp \cdot N$ $N = Number of inverters \qquad f = 2 tp \cdot N$ $T = 2 tp \cdot N$ $T = 2 tp \cdot N$ 20 ns (= tilH = to HL) $T = \frac{CV}{P}$ where $\Delta V = V_{00} - V_{M} = 1,65N$, for H_{PHL} where $\Delta V = V_{M} - 0 = 1,65V$, for H_{PLH} -AL Idy - T Jang F F 4,125 A M1 and My que saturated. Assume both from pps. G2 Transistor parameters = D,9 Ju Kh'= 196 MA/12 9,4 MA Vin = 0,743V * study M1 Z Isat Kn' (W Lett $I_{avg} = I_{sat} = \frac{l_{an}}{2} \left[\frac{W}{L_{aff}} \right] \left(V_{as} - V_{an} \right)^2 \iff V_{as} =$ $\frac{1}{19,6.10^{-6}(\frac{5}{0,3})} + 0,743$ = 1,01825, ... ~ 1,02 V Check if M1 was saturated: Vor - Vor - Im , No > Vo - Vrn, Vo > 1,02 - 0,343 = 0,259 (salvated most of 121 Hind)

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