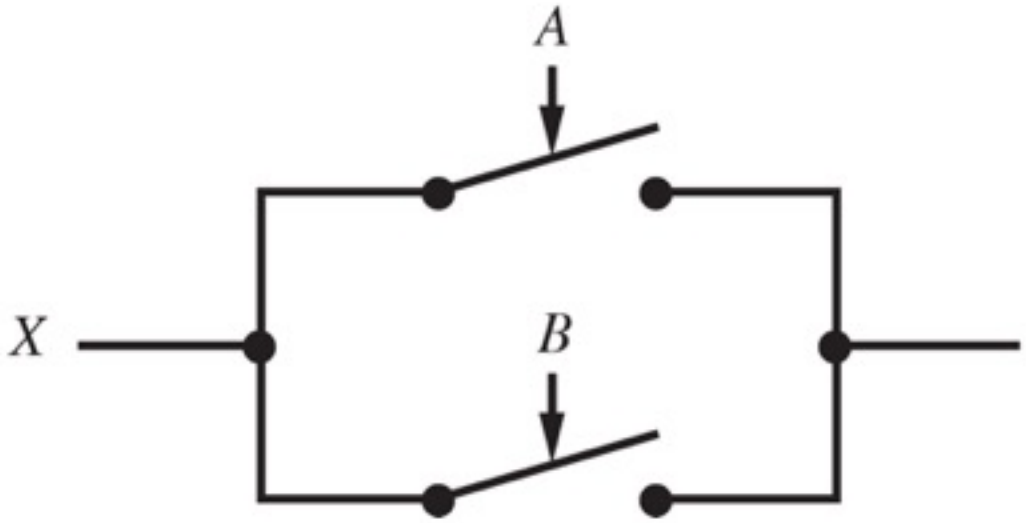
Digital ICs — Lectures

1) **Introduction** [Ch. 1]	*TSEI03/TSTE86*
2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
4) **Circuits** [Ch. 5]	*TSEI03/TSTE86*
5) **Combinational logic** [Ch. 6]	*TSEI03/TSTE86*
6) **Sequential circuits** [Ch. 7]	*TSEI03/TSTE86*
7) **Synchronization** [Ch. 10]	*TSTE86*
8) **Adders** [Ch. 11]	*TSEI03/TSTE86*
9) **Multipliers** [Ch. 11]	*TSTE86*
10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
11) **Manufacturing** [Ch. 2]	*TSTE86*
12) **System design** [Ch. 8]	*TSTE86*

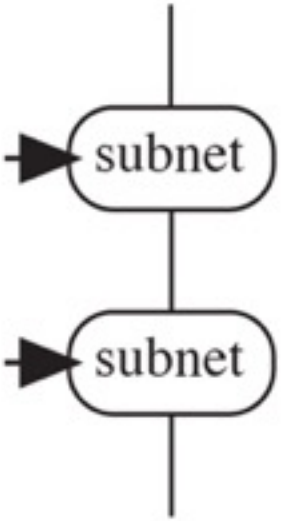
Switch Nets

X if $A \cdot B$
otherwise Z

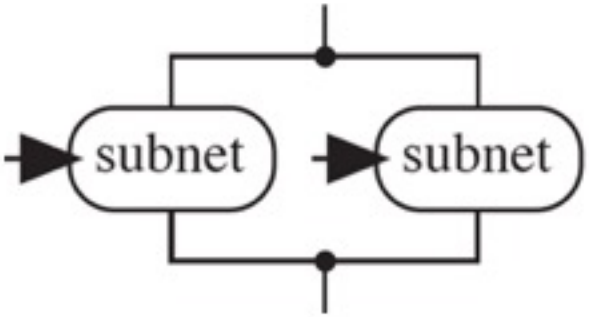


X if $A + B$
otherwise Z

Subnets

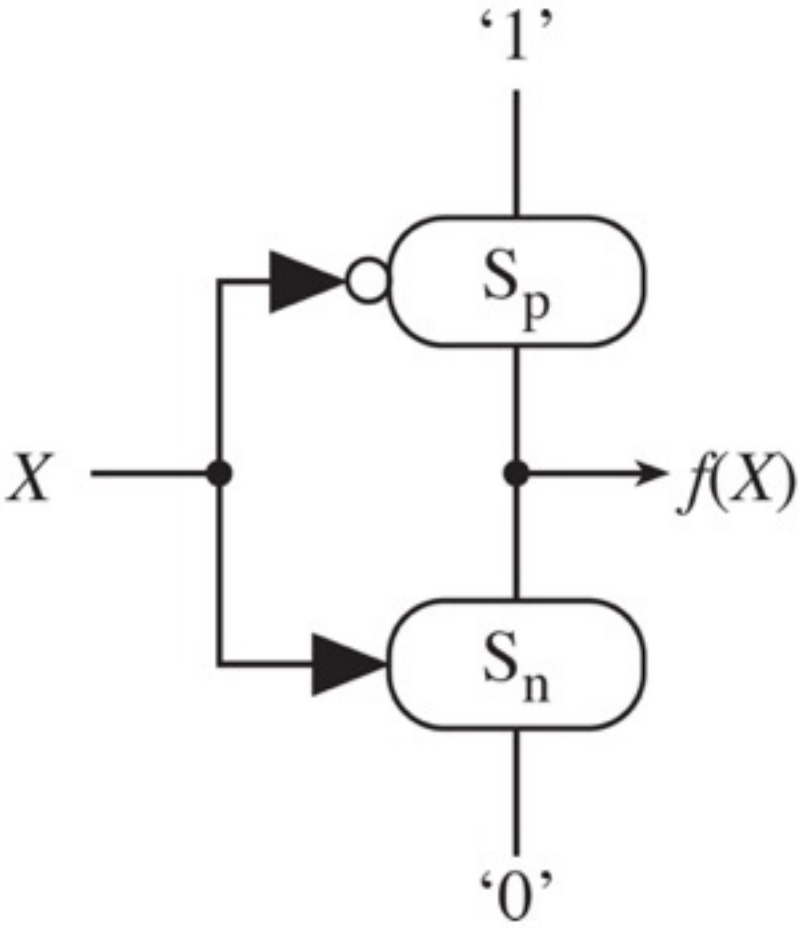


AND net
conducts when all subnets conduct



OR net
conducts when any subnet conducts

Static CMOS Switch Nets



Conducts when $f(\overline{X}) = 1$

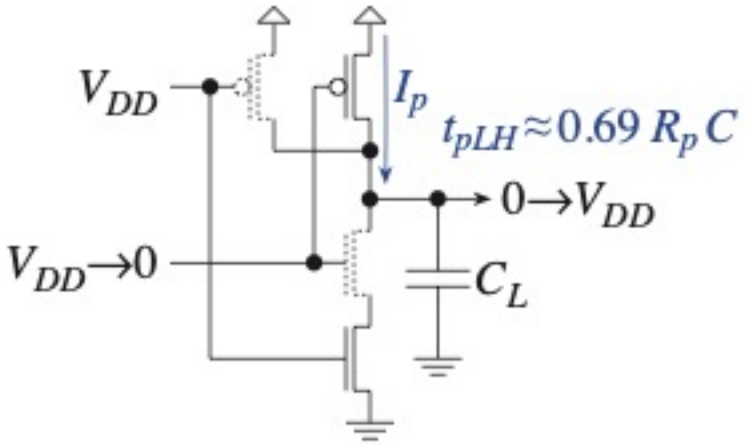
$$S_p = f\left(\overline{x_1}, \overline{x_2}, \ldots, \overline{x_m}\right)$$

Conducts when $f(X) = 0$

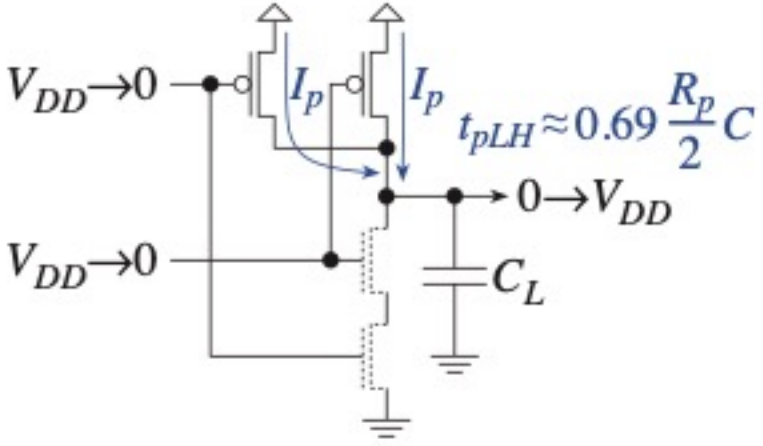
$$S_n = \overline{f\left(x_1, x_2, \ldots, x_m\right)}$$

Input Pattern Effects on Delay

Propagation delay of a NAND gate

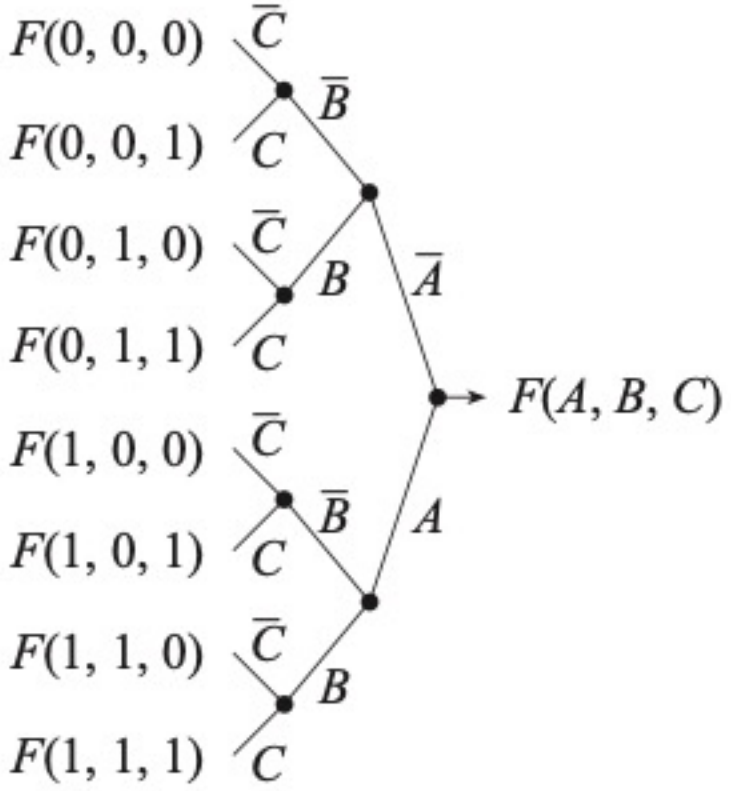


One input switches

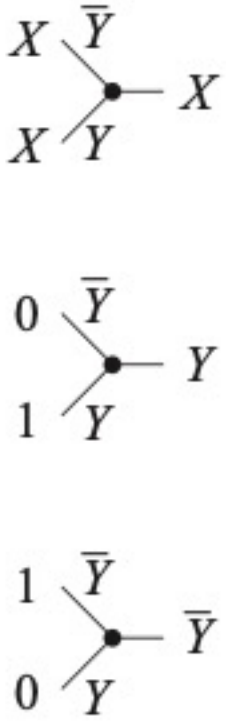


Two inputs switch

Designing Pass Transistor Logic

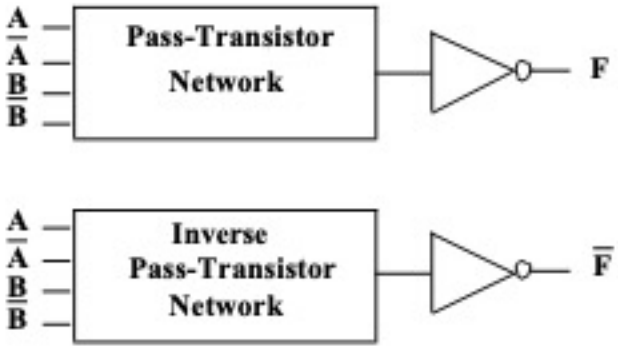


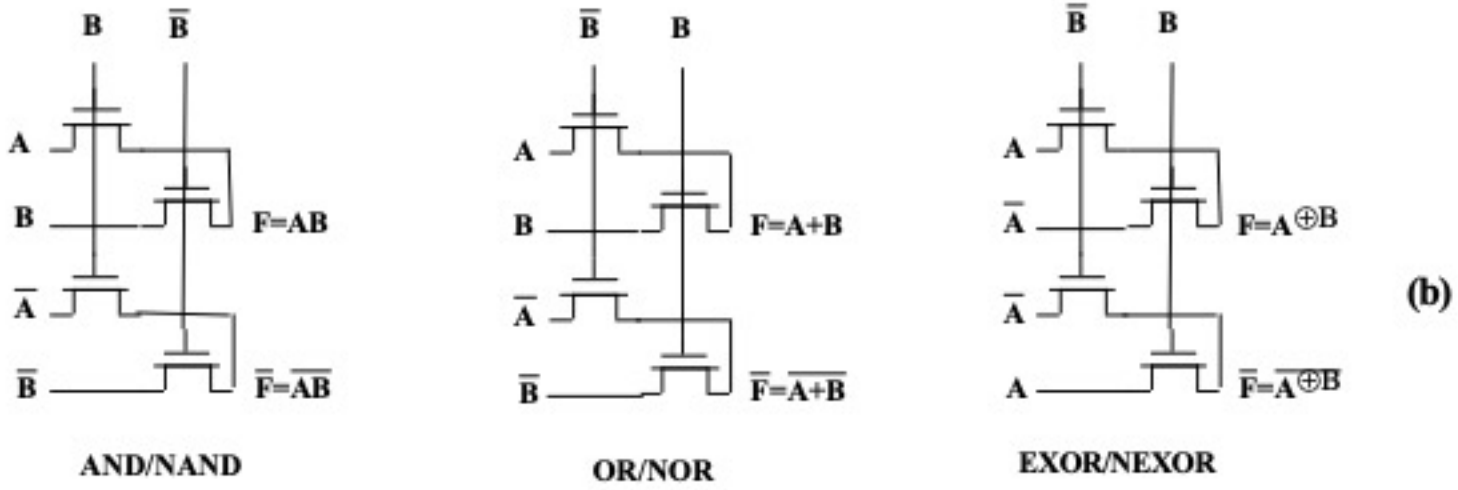
Start with binary tree



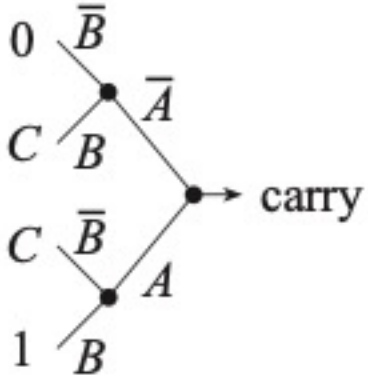
Simplify branches

Complementary Pass Transistor Logic

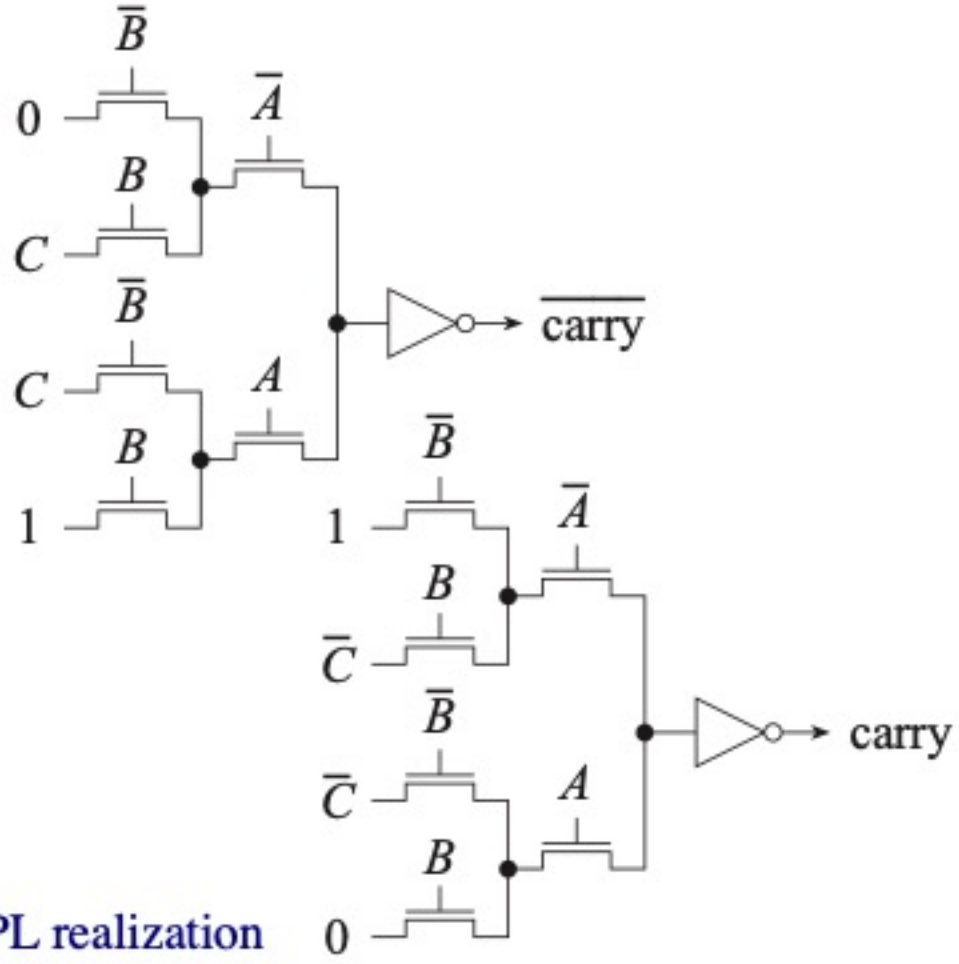




Carry Function in CPL

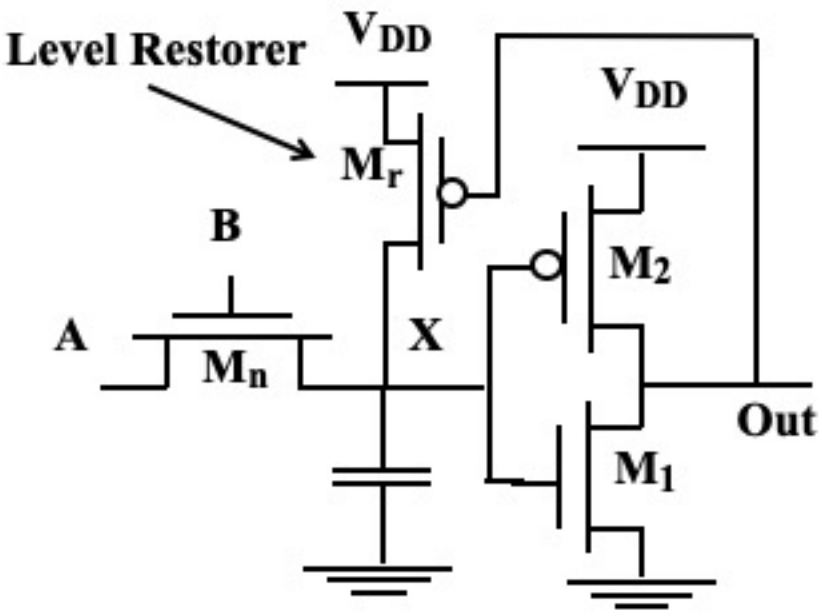


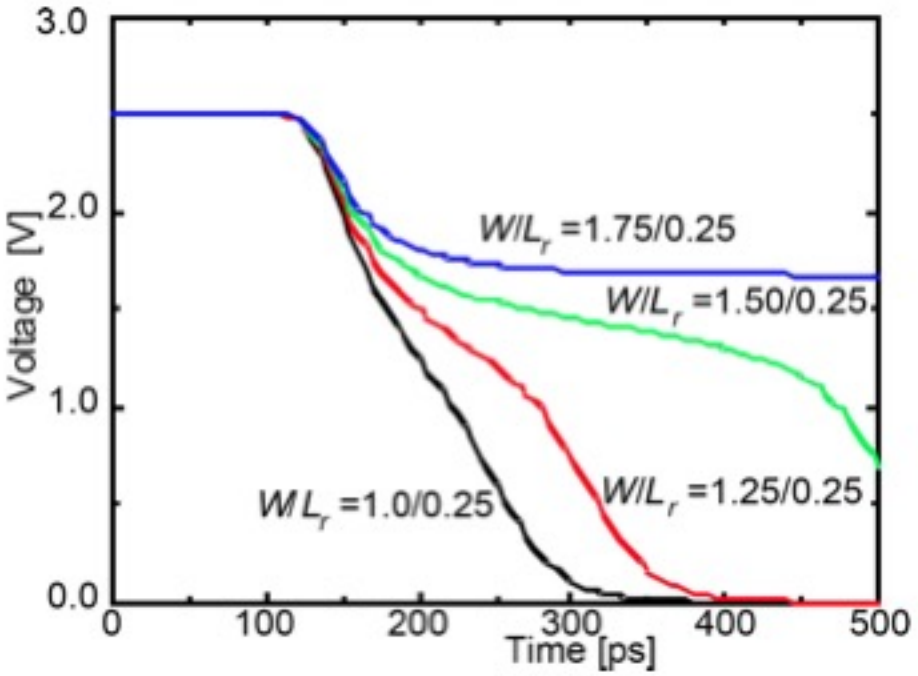
Binary carry tree



CPL realization

Level Restoring Transistor





Improved Switch: Transmission Gate