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Creative Uses of Block RAM

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All Virtex® and Spartan® FPGAs include many block RAMs. Even the smallest Virtex device has dozens of block RAMs, larger devices have hundreds, and the largest, the XC5VSX240T, has 1032. Because many designs do not require all of these block RAMs, this paper explores alternate uses for these functional blocks.

Read-Modify-Write, One Operation Per Clock

A synchronous RAM cannot perform read-modify-write operations in a single clock cycle, but the dual-port, synchronous block RAM in all Xilinx® FPGAs can pipeline the write operation and achieve a throughput of one read-modify-write operation per clock cycle. To do so, the designer uses Port A as the read port, uses Port B as the write port, and uses one common clock for both ports. The read address is routed to Port A. A copy of the read address is delayed by one clock and routed to Port B. The data from Port A is modified and used as the data input to Port B.

Shift Registers

A designer can use the read-before-write capability of a block RAM and an external counter to implement a shift register. A programmable counter (variable modulus) allows building a shift register of any length, and the shift register can operate at the full block RAM clock rate, which is more than 500 MHz. Here are some possible shift register configurations:

- One shift register 72 bits wide and up to 256 bits deep
    - Requires both ports of one 512 x 36 block RAM
    - Requires one 8-bit counter
    - The *MSB* of the address of Port A must be tied High to differentiate ports
    - The *MSB* of the address of Port B must be tied Low to differentiate ports
- One shift register 36 bits wide and up to 512 bits deep
    - Requires one port of one 512 x 36 block RAM
    - Requires one 9-bit counter
- One shift register 18 bits wide and up to 1024 bits deep
    - Requires one port of one 1K x 18 block RAM
    - Requires one 10-bit counter

Two, independent, half-length shift registers can be implemented by using both ports and two counters if the width is less than 72 bits.

Block RAM shift registers compare favorably with shift registers implemented with 16-bit Shift Register Look-up tables (SRL16s). The designer can use one block RAM plus one or two Configurable Logic Blocks (CLBs) to implement a shift register with a length of up to 18 Kbits. Using SRL16s in Virtex-4 FPGAs, it would take 140 CLBs to do the same. Therefore, if the design requires wide and deep shift registers, block RAM has the advantages of smaller size and lower power.

State Machines

Because block RAMs can be configured with any set of initial values, they make excellent dual-ported, registered ROMs that can be used as state machines. Figure 1 is an example of a simple Finite State Machine (FSM) with 1024 states, 10 outputs, and 4-way branching. It runs at up to 400 MHz and is implemented in a single block RAM.

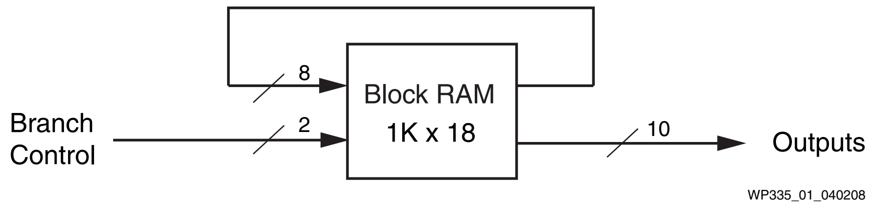

Figure 1: **Simple Finite State Machine**

The dual-ported memory shown in Figure 2 is divided into two, independent, half-size, single-port memories by tying the most significant bit (MSB) of the Port A address High and tying the MSB of the Port B address Low.

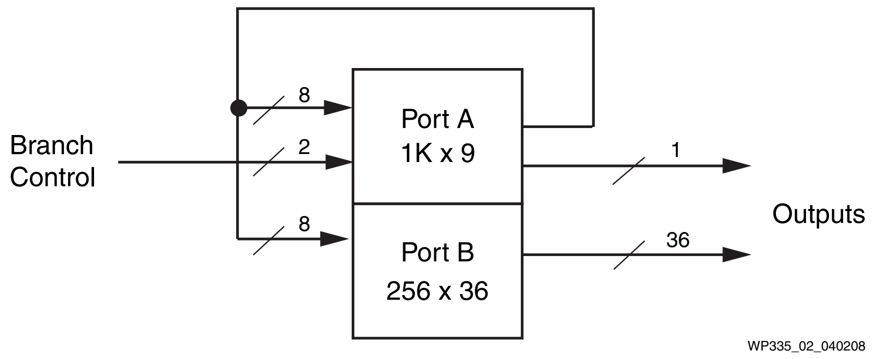

Figure 2: **FSM with Additional Outputs**

Port A is a 1K x 9 single-port RAM. Eight outputs are fed back as address inputs, providing 256 states and one output. The remaining two address inputs provide a four-way branch capability. Under the control of the two address inputs, any of the 256 states can conditionally branch to a set of four new states.

Port B is a 256 x 36 single-port RAM. It receives the same 8-bit state-defining address as Port A, and it has 36 outputs that can be defined for each state. The eighth address input can invoke an alternate definition of the 36 outputs. This design can be easily modified to provide 128 states with eight-way branching or 64 states with 16-way branching.

If additional branch-control inputs are needed, they can be combined in an input multiplexer as shown in Figure 3. The output from Port B in Figure 3 is delayed by one clock cycle relative to the output of Port A.

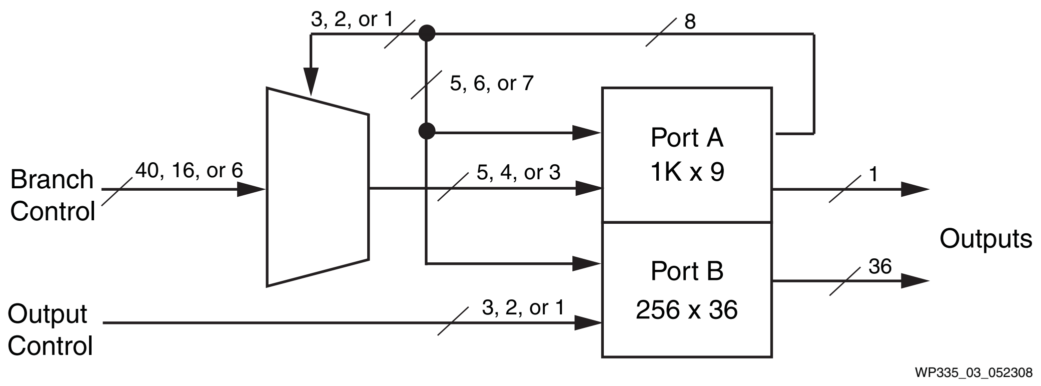

Figure 3: **FSM with Extended Branching**

The advantages of these FSM designs are low cost (no cost if the block RAM is not otherwise needed), high speed (400 MHz), the absence of layout or routing issues, and complete design freedom.

Other Uses of Block RAM

There are many other more specialized uses of block RAM, which include:

- A 20-bit binary counter or an 18-bit binary up-down counter
    - Uses one block RAM
    - Configured as 1K x 18
    - Runs at 400 MHz
- A 6-bit BCD counter that uses one port for the less significant half of the counter and the other port for the more significant half. This architecture is possible because the count algorithm, which is stored in the RAM, is common to both halves.
    - Uses one block RAM plus one CLB
    - Configured as 512 x 36
    - Runs at 400 MHz
- Two, independent, 11-bit-binary to 4-digit-BCD converters
    - Uses one block RAM
    - Configured as 1K x 18
    - LSBs do not pass through the converters
- Two, independent, 3-digit-BCD to 10-bit-binary converters
    - Uses one block RAM
    - Configured as 2K x 9
    - LSBs do not pass through the converters
- Sine-cosine look-up tables
    - One port for sine, the other port for cosine
    - 90°-shifted addresses
    - 8-bit amplitude
    - 10-bit angular resolution
- µ-law to/from A-law telephony code converter or µ/A-law to linear converter

Conclusion

Designers are encouraged to examine their Virtex and Spartan FPGA designs for surplus block RAM and to use these functions to unburden the FPGA logic. For example, using block RAM as state machines simplifies the design effort, significantly reduces routing overhead and power consumption, and achieves higher performance.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/04/08	1.0	Initial Xilinx release. Based on a previously published Tech Xclusive article by the same author.

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