



# 1164 PACKAGES QUICK REFERENCE CARD

Revision 2.2

()	Grouping	[]	Optional
{}	Repeated		Alternative
<b>bold</b>	As is	CAPS	User Identifier
<i>italic</i>	VHDL-93	c	commutative
b	::= BIT		
bv	::= BIT_VECTOR		
u/l	::= STD_ULOGIC/STD_LOGIC		
uv	::= STD_ULOGIC_VECTOR		
lv	::= STD_LOGIC_VECTOR		
un	::= UNSIGNED		
sg	::= SIGNED		
in	::= INTEGER		
na	::= NATURAL		
sm	::= SMALL_INT (subtype INTEGER range 0 to 1)		

## 1. IEEE's STD\_LOGIC\_1164

### 1.1 LOGIC VALUES

'U'	Uninitialized
'X'/'W'	Strong/Weak unknown
'0'/'L'	Strong/Weak 0
'1'/'H'	Strong/Weak 1
'Z'	High Impedance
'-'	Don't care

### 1.2 PREDEFINED TYPES

<b>STD_ULOGIC</b>	Base type
Subtypes:	
<b>STD_LOGIC</b>	Resolved STD_ULOGIC
<b>X01</b>	Resolved X, 0 & 1
<b>X01Z</b>	Resolved X, 0, 1 & Z
<b>UX01</b>	Resolved U, X, 0 & 1
<b>UX01Z</b>	Resolved U, X, 0, 1 & Z

**STD\_ULOGIC\_VECTOR**(na to | downto na)  
Array of STD\_ULOGIC

**STD\_LOGIC\_VECTOR**(na to | downto na)  
Array of STD\_LOGIC

## 1.3 OVERLOADED OPERATORS

Description	Left	Operator	Right
bitwise-and	u/l,uv,lv	<b>and, nand</b>	u/l,uv,lv
bitwise-or	u/l,uv,lv	<b>or, nor</b>	u/l,uv,lv
bitwise-xor	u/l,uv,lv	<b>xor, xnor</b>	u/l,uv,lv
bitwise-not		<b>not</b>	u/l,uv,lv

## 1.4 CONVERSION FUNCTIONS

From	To	Function
u/l	b	<b>TO_BIT</b> (from[, xmap])
uv,lv	bv	<b>TO_BITVECTOR</b> (from[, xmap])
b	u/l	<b>TO_STDULOGIC</b> (from)
bv,uv	lv	<b>TO_STDLOGICVECTOR</b> (from)
bv,lv	uv	<b>TO_STDULOGICVECTOR</b> (from)

## 2. IEEE's NUMERIC\_STD

### 2.1 PREDEFINED TYPES

<b>UNSIGNED</b> (na to   downto na)	Array of STD_LOGIC
<b>SIGNED</b> (na to   downto na)	Array of STD_LOGIC

### 2.2 OVERLOADED OPERATORS

Left	Op	Right	Return
	<b>abs</b>	sg	sg
	-	sg	sg
un	<b>+, -, *, /, rem, mod</b>	un	un
sg	<b>+, -, *, /, rem, mod</b>	sg	sg
un	<b>+, -, *, /, rem, mod<sub>c</sub></b>	na	un
sg	<b>+, -, *, /, rem, mod<sub>c</sub></b>	in	sg
un	<b>&lt;, &gt;, &lt;=, &gt;=, /=</b>	un	bool
sg	<b>&lt;, &gt;, &lt;=, &gt;=, /=</b>	sg	bool
un	<b>&lt;, &gt;, &lt;=, &gt;=, /=<sub>c</sub></b>	na	bool
sg	<b>&lt;, &gt;, &lt;=, &gt;=, /=<sub>c</sub></b>	in	bool

### 2.3 PREDEFINED FUNCTIONS

<b>SHIFT_LEFT</b> (un, na)	un
<b>SHIFT_RIGHT</b> (un, na)	un
<b>SHIFT_LEFT</b> (sg, na)	sg
<b>SHIFT_RIGHT</b> (sg, na)	sg
<b>ROTATE_LEFT</b> (un, na)	un
<b>ROTATE_RIGHT</b> (un, na)	un
<b>ROTATE_LEFT</b> (sg, na)	sg
<b>ROTATE_RIGHT</b> (sg, na)	sg
<b>RESIZE</b> (sg, na)	sg
<b>RESIZE</b> (un, na)	un
<b>STD_MATCH</b> (u/l, u/l)	bool
<b>STD_MATCH</b> (uv, uv)	bool
<b>STD_MATCH</b> (lv, lv)	bool
<b>STD_MATCH</b> (un, un)	bool
<b>STD_MATCH</b> (sg, sg)	bool

## 2.4 CONVERSION FUNCTIONS

From	To	Function
un,lv	sg	<b>SIGNED</b> (from)
sg,lv	un	<b>UNSIGNED</b> (from)
un,sg	lv	<b>STD_LOGIC_VECTOR</b> (from)
un,sg	in	<b>TO_INTEGER</b> (from)
na	un	<b>TO_UNSIGNED</b> (from, size)
in	sg	<b>TO_SIGNED</b> (from, size)

## 3. IEEE's NUMERIC\_BIT

### 3.1 PREDEFINED TYPES

<b>UNSIGNED</b> (na to   downto na)	Array of BIT
<b>SIGNED</b> (na to   downto na)	Array of BIT

### 3.2 OVERLOADED OPERATORS

Left	Op	Right	Return
	<b>abs</b>	sg	sg
	-	sg	sg
un	<b>+, -, *, /, rem, mod</b>	un	un
sg	<b>+, -, *, /, rem, mod</b>	sg	sg
un	<b>+, -, *, /, rem, mod<sub>c</sub></b>	na	un
sg	<b>+, -, *, /, rem, mod<sub>c</sub></b>	in	sg
un	<b>&lt;, &gt;, &lt;=, &gt;=, /=</b>	un	bool
sg	<b>&lt;, &gt;, &lt;=, &gt;=, /=</b>	sg	bool
un	<b>&lt;, &gt;, &lt;=, &gt;=, /=<sub>c</sub></b>	na	bool
sg	<b>&lt;, &gt;, &lt;=, &gt;=, /=<sub>c</sub></b>	in	bool

### 3.3 PREDEFINED FUNCTIONS

<b>SHIFT_LEFT</b> (un, na)	un
<b>SHIFT_RIGHT</b> (un, na)	un
<b>SHIFT_LEFT</b> (sg, na)	sg
<b>SHIFT_RIGHT</b> (sg, na)	sg
<b>ROTATE_LEFT</b> (un, na)	un
<b>ROTATE_RIGHT</b> (un, na)	un
<b>ROTATE_LEFT</b> (sg, na)	sg
<b>ROTATE_RIGHT</b> (sg, na)	sg
<b>RESIZE</b> (sg, na)	sg
<b>RESIZE</b> (un, na)	un

### 3.4 CONVERSION FUNCTIONS

From	To	Function
un,bv	sg	<b>SIGNED</b> (from)
sg,bv	un	<b>UNSIGNED</b> (from)
un,sg	bv	<b>BIT_VECTOR</b> (from)
un,sg	in	<b>TO_INTEGER</b> (from)
na	un	<b>TO_UNSIGNED</b> (from)
in	sg	<b>TO_SIGNED</b> (from)

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