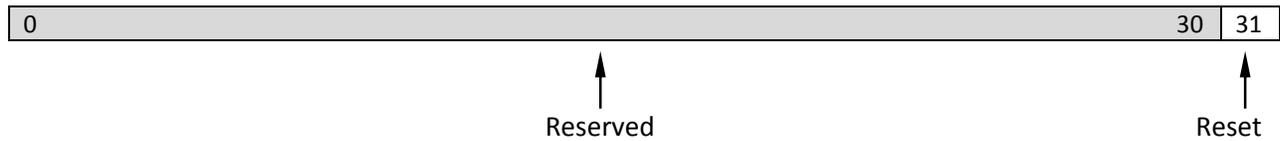
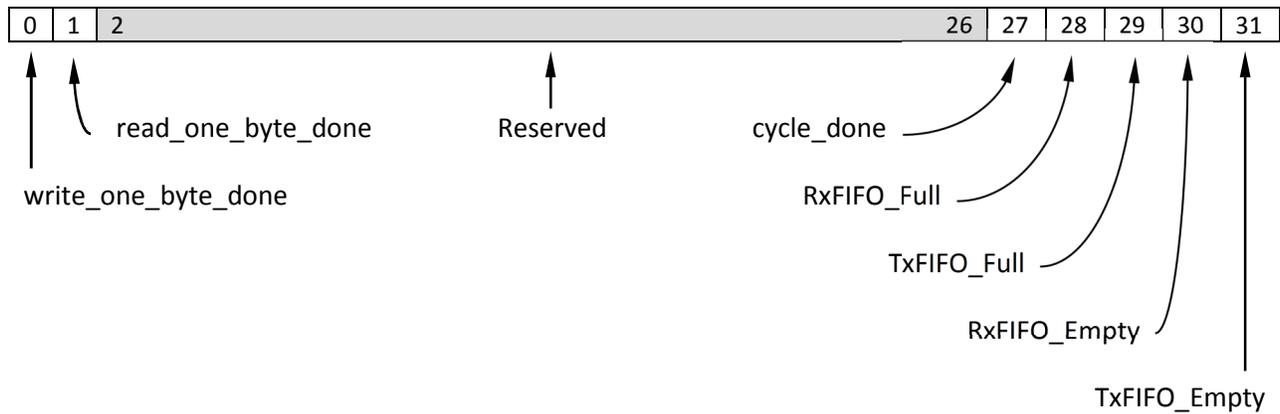


## Reset Register: RESET\_REG

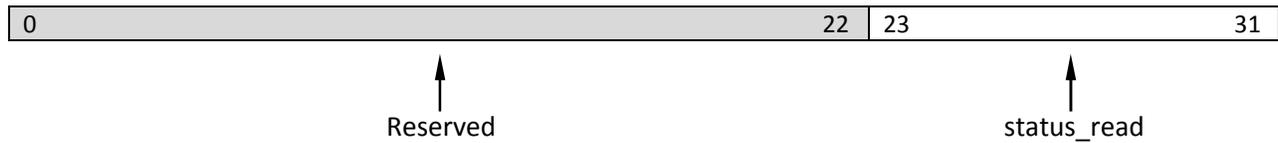


## Status Register: STATUS\_REG



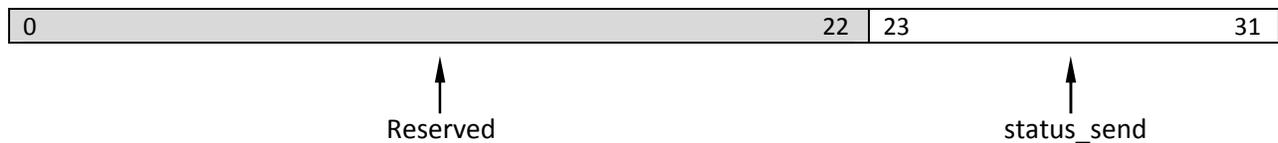
| Bits | Name                | Description   | Reset Value |
|------|---------------------|---|-------------|
| 0    | write_one_byte_done | Writing one Byte to Transmit FIFO is done<br>0 Reading one Byte in progress<br>1 Reading one Byte done  | 1           |
| 1    | read_one_byte_done  | Reading one Byte from Receive FIFO is done<br>0 Writing one Byte in progress<br>1 Writing one Byte done | 1           |
| 2-26 | Reserved            | Not used  | 0           |
| 27   | cycle_done          | A cycle process is done<br>0 While working<br>1 When done   | 1           |
| 28   | RxFIFO_Full         | Indicates that the receive FIFO is full<br>0 Receive FIFO is not full<br>1 Receive FIFO is full         | 0           |
| 29   | TxFIFO_Full         | Indicates that the transmit FIFO is full<br>0 Transmit FIFO is not full<br>1 Transmit FIFO is full      | 0           |
| 30   | RxFIFO_Empty        | Indicates that the receive FIFO is empty<br>0 Receive FIFO is not empty<br>1 Receive FIFO is empty      | 1           |
| 31   | TxFIFO_Empty        | Indicates that the transmit FIFO is empty<br>0 Transmit FIFO is not empty<br>1 Transmit FIFO is empty   | 1           |

### Occupancy on receive FIFO Register: OCCUPANCY\_RXFIFO\_REG



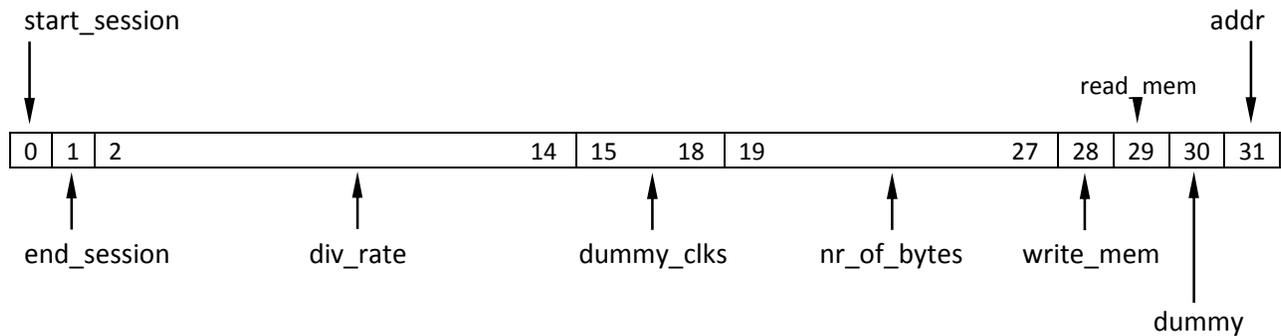
| Bits  | Name        | Description   | Reset Value |
|-------|-------------|---|-------------|
| 0-22  | Reserved    | Not used  | 0           |
| 23-31 | status_read | Indicates the number of Bytes written onto receive FIFO. Its maximum value can be 100h. | 1           |

### Occupancy on transmit FIFO Register: OCCUPANCY\_TXFIFO\_REG



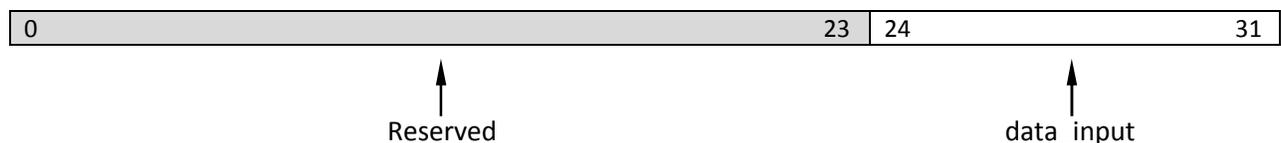
| Bits  | Name        | Description   | Reset Value |
|-------|-------------|---|-------------|
| 0-22  | Reserved    | Not used  | 0           |
| 23-31 | status_send | Indicates the number of Bytes written onto transmit FIFO. Its maximum value can be 104h, when transmit FIFO is also full. | 1           |

## Control cycle Register: CONTROL\_CYCLE\_REG

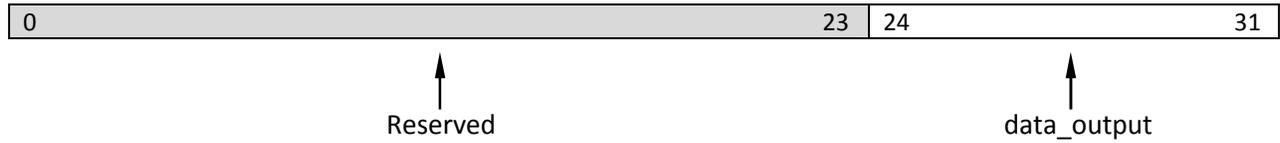


| Bits  | Name          | Description   | Reset Value |
|-------|---------------|---|-------------|
| 0     | start_session | 1 starts a new cycle session<br>0 resets internal latches (but not disables the currently running cycle session)  | 0           |
| 1     | end_session   | 1 when used in conjunction with the following types of cycles: <ul style="list-style-type: none"> <li>- command -&gt; end</li> <li>- command + address -&gt; end</li> <li>- command + dummy -&gt; end</li> <li>- command + address + dummy -&gt; end</li> </ul> 0 in all other types of cycles (they automatically go to end) | 0           |
| 2-14  | div_rate      | The division rate for the Serial Clock (C).   | 0           |
| 15-18 | dummy_clks    | Number of dummy bits.   | 0           |
| 19-27 | nr_of_bytes   | Number of Bytes to read/write from/to Serial Flash Memory.  | 0           |
| 28    | write_mem     | Write to Serial Flash Memory.   | 0           |
| 29    | read_mem      | Read from Serial Flash Memory.  | 0           |
| 30    | dummy         | Send dummy bits (high impedance).   | 0           |
| 31    | addr          | Send the Address.   | 0           |

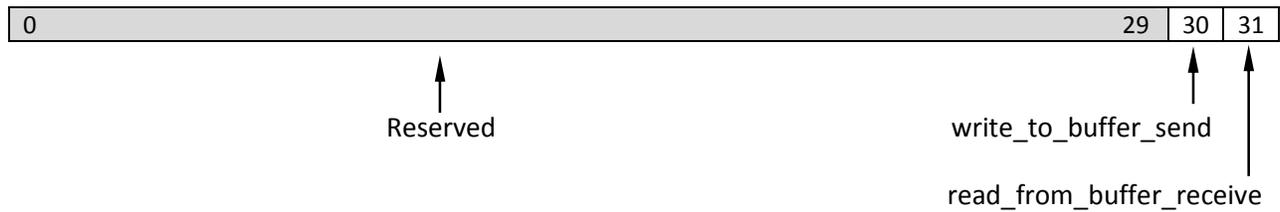
## Data input Register: DATA\_IN\_REG



### Data output Register: DATA\_OUT\_REG

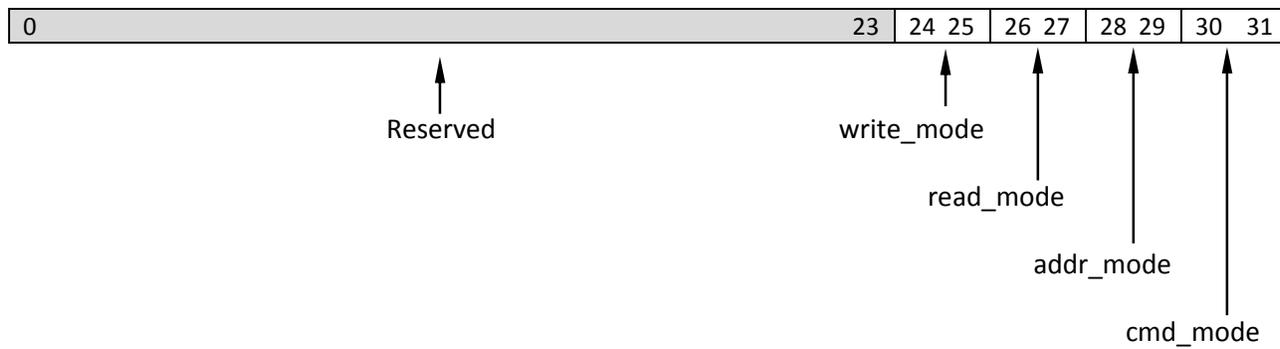


### Control for FIFO Register: CONTROL\_FIFO\_REG



| Bits | Name                     | Description   | Reset Value |
|------|--------------------------|---|-------------|
| 0-29 | Reserved                 | Not used  | 0           |
| 30   | write_to_buffer_send     | 1 Enables one Byte writing to transmit FIFO<br>0 Resets internal latches  | 0           |
| 31   | read_from_buffer_receive | 1 Enables one Byte reading from receive FIFO<br>0 Resets internal latches | 0           |

### Operating Modes Register: MODES\_REG



| Bits  | Name       | Description   | Reset Value |
|-------|------------|---|-------------|
| 0-23  | Reserved   | Not used  | 0           |
| 24-25 | write_mode | Mode on which writing will be made<br>0 Extended Mode<br>1 Dual Mode<br>2 Quad Mode                 | 0           |
| 26-27 | read_mode  | Mode on which reading will be made<br>0 Extended Mode<br>1 Dual Mode<br>2 Quad Mode                 | 0           |
| 28-29 | addr_mode  | Mode on which the address will be send<br>0 Extended Mode<br>1 Dual Mode<br>2 Quad Mode             | 0           |
| 30-31 | cmd_mode   | Mode on which the command instruction will be send<br>0 Extended Mode<br>1 Dual Mode<br>2 Quad Mode | 0           |

| Register             | Offset          |
|----------------------|-----------------|
| RESET_REG            | BASEADDR + 0x00 |
| STATUS_REG           | BASEADDR + 0x04 |
| OCCUPANCY_RXFIFO_REG | BASEADDR + 0x08 |
| OCCUPANCY_TXFIFO_REG | BASEADDR + 0x0C |
| CONTROL_CYCLE_REG    | BASEADDR + 0x10 |
| DATA_IN_REG          | BASEADDR + 0x14 |
| DATA_OUT_REG         | BASEADDR + 0x18 |
| CONTROL_FIFO_REG     | BASEADDR + 0x1C |
| MODES_REG            | BASEADDR + 0x20 |