TSEA26 Tutorial 5. Address Generation Units

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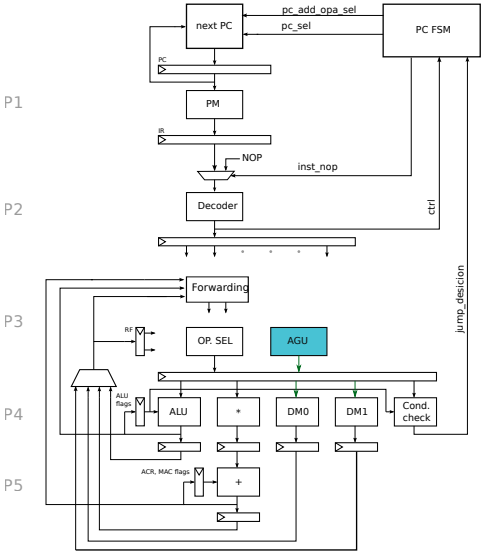
Address Generation Units (AGUs)



- Hardware for computing addresses for the data memories
- Inputs:
  - Decoded instructions
  - Data from RF
  - Data in Address Register
- Outputs:
  - Addresses for data memories
  - New values for Address Registers

Why?

- Memory addressing and compute are often independent
- Allows offloading of task from ALU
- Allows computation in parallel with ALU and MAC
- `sum += DM0[ptr0++] * DM1[ptr1++]` in a single cycle

Addressing Modes

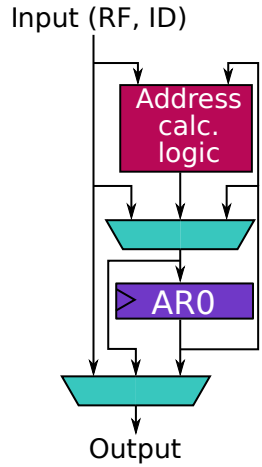
Examples of addressing modes

Name	**Description**	**Example**
Direct	$A \Leftarrow$ Constant from instruction	`ld r0, (5)`
Register indirect	$A \Leftarrow$ Value from register	`ld r0, (r1)`
Index	$A \Leftarrow$ `arX` + value from register	`ld r0, (ar0, r1)`
	$A \Leftarrow$ `arX` + constant	`ld r0, (ar0, 5)`
Post increment/decremnt	$A \Leftarrow$ `arX`, `arX` $\Leftarrow$ `arX` $+ 1$	`ld r0, (ar0++)`
Variable post increment	$A \Leftarrow$ `arX`, `arX` $\Leftarrow$ `arX` $+ STEP$	`ld r0, (ar0+=STEP)`
...		

Lots of more options: modulo addressing, pre-increment, whatever suits your program

General AGU structure

- General structure with a single address register
- Address calculation unit for computing next ACR value
  - Adder for incremental addressing
  - Top/bot/step registers
- A bit more complexity with multiple ARs



Exercises

- Exercise 5.1 to 5.3