Skriftlig tentamen, TMEL53
Digitalteknik M, 2017-06-07

Vid godkänd dugga X behöver du ej göra uppgift X, för $X = 1,\ 2,\ 3$.

1. (a) Omvandla det decimala talet 1.75 till ett binärt tal. Markera binärpunkten. (1 p)

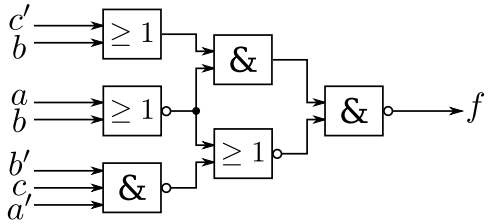
   (b) Omvandla det decimala talet -11 till ett binärt tal i tvåkomplementsrepresentation. (2 p)

   (c) De binära talen 01000111_2 och 1110101_2 ska adderas **binärt**. Utför additionen **binärt** under förutsättning att bägge talen är positiva, dvs i vanlig binär representation. (3 p)

   (d) Omvandla 567_8 till ett decimalt tal. (1 p)

   (e) Beräkna $17 - 11$ genom att representera bägge talen i lämpligt binärt format och utföra beräkningen med en **binär addition**, dvs beräkna $17 + (-11)$. (3 p)

2. (a) Bestäm ett förenklat uttryck för f givet följande krets (4 p)

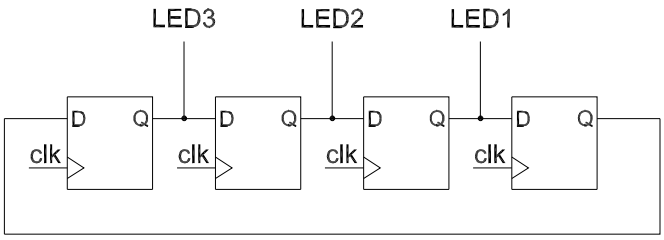


   (b) Följande sanningstabell är given. Konstruera och rita en kombinatorisk krets f. De grindar som finns att tillgå är tvåingångars AND-grindar, tvåingångars OR-grindar samt inverterare. För full poäng skall kretsen använda ett minimalt antal grindar och inverterare. (4 p)

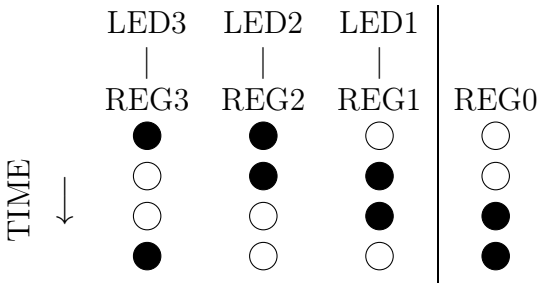
a	b	c	d	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	-
0	0	1	1	-
0	1	0	0	1
0	1	0	1	-
0	1	1	0	-
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	-
1	0	1	1	0
1	1	0	0	0
1	1	0	1	-
1	1	1	0	1
1	1	1	1	1

   (c) Konstruera en treingångars NAND-grind med enbart tvåingångars NAND-grindar. (2 p)

3. The red light of our bike has three LEDs. In one of the modes, the light seems to flow from left to right. One way to do it is to use four D flip-flops that form a shift register:



If these registers are loaded with the values 1,1,0,0, the light will flow cyclically according to:



(a) Modify the circuit to add an input signal LOAD. If this signal is active, the sequence 1,1,0,0 is loaded into the registers. If LOAD is not active, the registers move data cyclically. Add only logic gates. (3 p)

(b) We want to reduce the number of registers. Design another solution to the same problem (including the LOAD signal) that uses only two registers. (5 p)

(c) Which advantages of each solutions can you figure out? Discuss 2 advantages, 1 per solution. Think broadly. Reason your answer. (2 p)

4. Konstruera en krets med insignaler $x = (x_3, x_2, x_1, x_0)$ och utsignaler $u = (u_3, u_2, u_1, u_0)$ där båda vektorerna ska tolkas som ett binärt tal där högst index i båda fallen motsvarar mest signifikant bit. Utvärdet u ska vara den multiplikativa inversen modulo 11 till x, dvs det u som löser

$$x \cdot u \equiv 1 \bmod 11$$

Till exempel om

$$x = 0010_2 = 2_{10} \Rightarrow u = 6_{10} = 0110_2$$

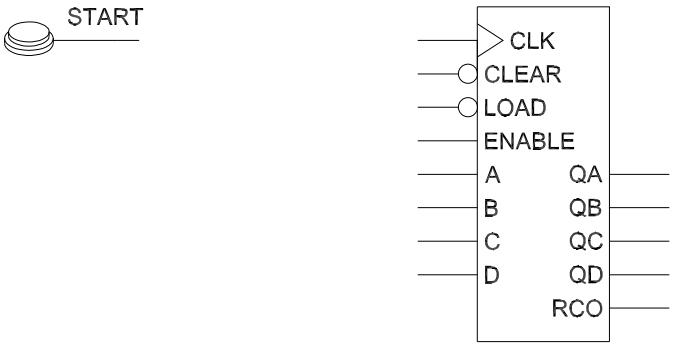
eftersom $2 \cdot 6 = 12 \equiv 1 \bmod 11$. De multiplikativa inverserna modulo 11 är

x	u
1	1
2	6
3	4
4	3
5	9

x	u
6	2
7	8
8	7
9	5
10	10

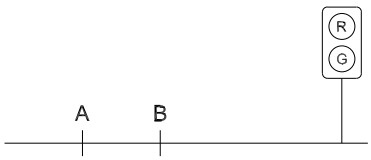
För $x \in \{0, 11, 12, 13, 14, 15\}$ så spelar det ingen roll vad u blir. Konstruera kretsen med NAND-grindar och inverterare (insignalernas inverser är ej tillgängliga). Så få grindar som möjligt ska användas. (10 p)

5. The circuit in the figure is a 4-bit binary counter. We want to use it to count $1, 2, 2, 3, 4, 4, 5, 6, 6, 1, 2, 2, \ldots$ The button START allows us to initialize the counter: After we push the button, the counter will be set to 1 (the first number of the sequence) in the next clock cycle. Assume that we keep the button pushed during several clock cycles. After we release the button, the counter will continue with the sequence, i.e., it will go to 2 (the second number of the sequence) in the next clock cycle after the button is released, and so on. Apart from the counter, you can use two D flip-flops and any number of logic gates to achieve this behavior. Include all the design steps and reason your solution. You can use your knowledge about state machines for this exercise. D and QD are the MSBs. The priority of the control signals is CLEAR > LOAD > ENABLE.



(10 p)

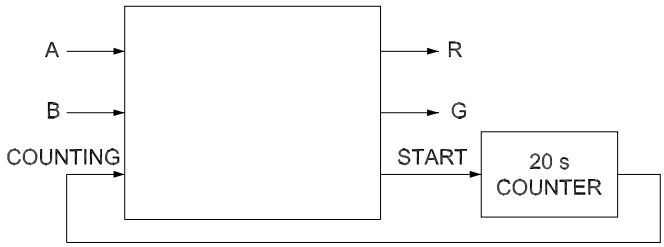
6. In Linköping, the traffic lights for bicycles are controlled by two sensors on the ground (A and B in the figure). The traffic light changes color after the bicycle has crosses the sensors. We consider that a bike crosses the sensors when the sequence "00", "10", "11", "01änd "00"is received in [AB]. Note that each of the steps of the sequence may be active for more than one clock cycle. For instance, "00", "10", "10", "10", "11", "11", "01", "00"is also a valid sequence.



Initially the traffic light is in red (R). After the sequence is received, it goes to green (G) for 20 seconds. Then, it goes back to red. The traffic light is only activated if A and B are crossed while the traffic light is in red, i.e., bikes can pass over the sensors while the traffic light is in green and this does not make the traffic light be activated again. Furthermore, we consider that only one bike can be over the sensors A and B at the same time. Finally, if an incorrect sequence is received, the system starts to search the sequence from the beginning.

To build the system, we make use of a counter that counts 20s. It only has an input signal, START. When it is active, it starts the count. The output is the signal COUNTING, which is active for the 20s of the count and then it goes to '0' until START is activated again.

The system will look like the figure below and it will include a state machine.



(a) Draw the state diagram (tillståndsdiagram) of the state machine. (3 p)

(b) Obtain the logic function of the outputs (R, G, START) as a function of the inputs (A, B, COUNTING) and the states of the state machine. (3 p)

(c) Draw the circuit. (2 p)

(d) The 20 s counter works at $f_{\mathrm{CLK}} = 50$ MHz. How many bits does this counter need to have? (2 p)