Applikationsspecifika Integrerade kretsar

Tentamen

TSTE81

för Y4, D4 och TE

Tid:	Onsdag 1 September 1997 kl. 14.00 - 18.00
Plats:	Kårallen
Ansvarig lärare:	Kent Palmkvist, 281347
Hjälpmedel:	Räknedosa, Formelsamling i Aktiva och Tidsdiskreta filter, Formelsamling i kretsteori samt allmänna tabellverk.
Anvisningar:	För godkänd tentamen fordras ca 30 poäng
Visning:	Tisdag 16 September 1997 kl. 13.00-14.00 (Kent Palmkvists tjänsterum)
Lösningar:	Anslås på Systemtekniks anslagstavla i labkorridoren
Betygslista:	Anslås senast 1997-09-15 på anslagstavlan i labkorridoren

1. a) How fast grows the size of a distributed arithmetic unit when the number of inputs are increased? (2)

   b) How many clock cycles is needed for a multiplier implemented using Booth's algorithm compared to using an ordinary shift-accumulator? (2)

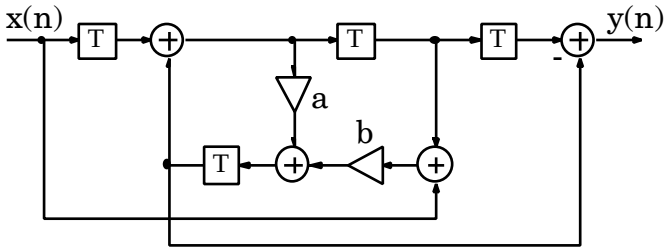
   c) What is sign-magnitude truncation? (2)

   d) What difference is there between a preemptive and non-preemptive processing element? (2)

   e) Why is it more important to generate a correct design when using ASICs compared to a standard DSP solution? (2)

2. The filter below is implemented using an isomorphic mapping to bit-serial arithmetic. The data wordlength is 14 bits. Multiplier a has a latency of 5 clock cycles, multiplier b has a latency of 7 clock cycles, and the additions has a latency of 1 clock cycle. The clock frequency is 150 MHz, and the sample rate is 5 MHz.

   Introduce shimming delays. (8)



3. The recursive filter above is implemented using homogenous non-preemptive processing elements. Multiplication a requires 5 clock cycles, multiplication b requires 7 clock cycles, and addition requires 1 clock cycle.

   a) What is the minimal sample period? (4)

   b) Estimate the minimal number of resources required if the sample period is equal to the minimal sample period. (4)

   c) Draw the precedence graph. (6)

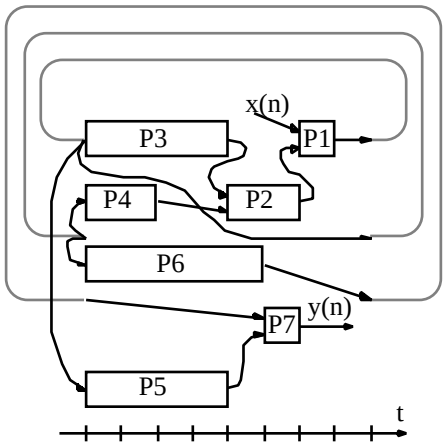
   d) Schedule the algorithm to reach the minimal sample period. (6)

4. The schedule below is implemented using non-homogenous non-preemptive processing elements. Processes P1 and P7 are of the same type, and processes P2, P3, and P5 are of the same type.

a) Perform processing element resource allocation and assignment using clique partitioning. (6)

b) Draw a variable lifetime diagram. (4)

c) Perform memory cell resource allocation and assignment using the left edge algorithm. Indicate the steps performed in the allocation/assignment. Variables cannot be assigned edge-to-edge, and are not allowed to overlap themselves. (6)



5. A multiplication by a constant -1.1875 is to be implemented. The input data wordlength is 15 bits.

a) Draw the non-optimized logic diagram of the multiplier. Use blocks such as full adders, flip-flops etc. (4)

b) Optimize the structure. (3)

c) What is the latency measured in clock cycles for the multiplier? (2)

d) What is the throughput measured in clock cycles for the multiplier? (2)

e) Implement the multiplication using 2 or less fulladders. Hint: -1.1875 = –1 – 0.25 + 0.0625. (5)