Applikationsspecifika Integrerade kretsar

Tentamen
TSTE81

för Y4, D4 och TE

Tid:	Onsdag 7 Maj 1997 kl. 14.00 - 18.00
Plats:	U1, U4
Ansvarig lärare:	Kent Palmkvist, 281347 eller 070 5762095
Hjälpmedel:	Räknedosa, Formelsamling i Aktiva och Tidsdiskreta filter, Formelsamling i kretsteori samt allmänna tabellverk.
Anvisningar:	För godkänd tentamen fordras ca 30 poäng
Visning:	Torsdag 22 Maj 1997 kl. 13.00-14.00 (Lars Wanhammars tjänsterum)
Lösningar:	Anslås på Systemtekniks anslagstavla i labkorridoren
Betygslista:	Anslås senast 1997-05-22 på anslagstavlan i labkorridoren

1. a) How costly in terms of additions/subtractions is it to check what sign a SDC number has? (2)

    b) Does an isomorphic mapping always result in optimal resource utilization? Motivate your answer. (2)

    c) Draw the principal structure of an harvard architecture using ALU, memories, control units etc as building blocks. (2)

    d) How is the propagation delay affected by an increase in junction temperature? (2)

    e) Name two layout styles used for ASIC chips. (2)

2. The structure below is implemented using bitserial arithmetic. The multiplier coefficients are represented in two's complement with 5 fractional bits and the data wordlength is 12 bits. A static logic style is used, with operations containing only the required flip-flops. The multipliers are serial/parallel type using signextension to avoid sign subtraction.

    a) What is the latency expressed in clock cycles? (4)

    b) What is the throughput of the structure? (4)
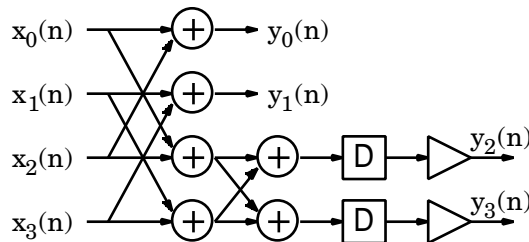
3. An algorithm is implemented using 3 distributed arithmetic units. Each distributed arithmetic unit has 5, 9, and 3 inputs respectively. A shift-ackumulator uses 0.1 mm^2 and a N word ROM uses $0.005 * 2^N$ mm^2.

    a) Suggest a structure which results in a design using less than 1.3 mm^2 of silicon area. Time-multiplexing of elements are not allowed. (5)

    b) Optimization of the coefficients in the first distributed arithmetic unit makes it possible to have a ROM length of 8 bits including sign and the four bits in the middle of the coefficient always set to 0110. Draw the simplified shift-ackumulator structure due to these simplifications. (5)
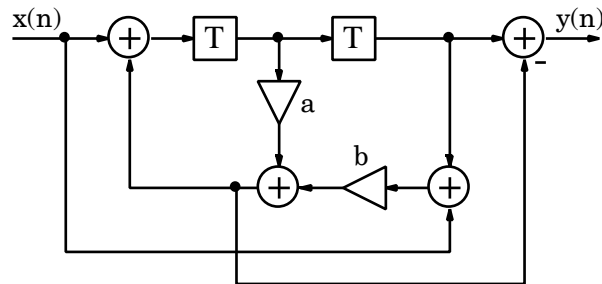
4. The filter structure below is to be implemented.

   a) Draw the precedence graph of the algorithm. (6)

   b) Write down the operations in computational order. Simplify the description. (4)

   c) Perform an ALAP schedule of the operations. (4)

   d) Introduce pipelining into the original structure. The critical path must at most contain one multiplication and two additions. (4)

5. The channel equalizer of transversal FIR type shown below is to be implemented. 2-input additions requires 2 clock cycles, and multiplications 4 clock cycles. The clock frequency is 20 MHz and the required sample period is 500 kHz.

   a) Compute the minimal sample period T_{min}. (4)

   b) Estimate the required number of adders and multipliers for a filter with 4 filter taps. Non-homogenous processing elements with latency = 1/throughput are used. (4)
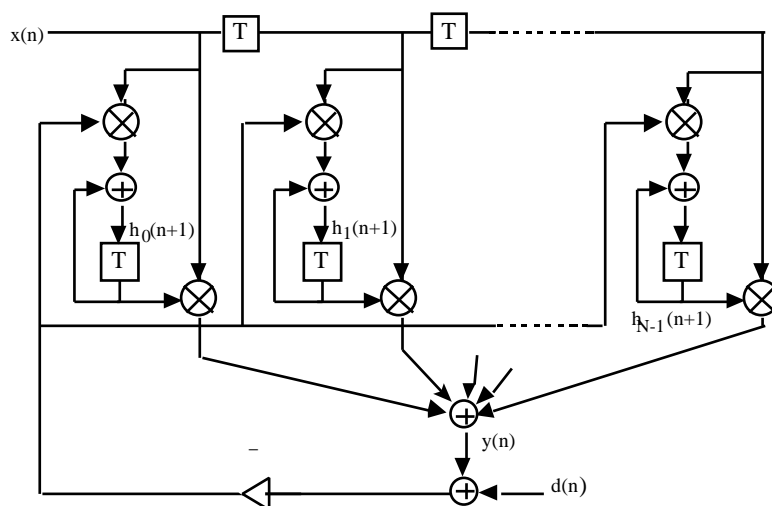
6. An integrator ($y(n) = y(n-1) + x(n)$) is built using two's complement representation.

   a) Draw the principal output if a unit step is put on its input. (2)

   b) What is the output in the same situation if saturation logic is used? (2)

7. The schedule below is to be mapped onto a shared memory hardware.

   a) Determine the process allocation and assignment using clique partitioning. Indicate the main steps of the algorithm. Homogenuous processing elements are used. (4)

   b) Draw a lifetime diagram for the variables. (4)

   c) Allocate and assign memory cells to the variables using the left edge algorithm. Indicate the main steps in the algorithm. Assume that variables cannot be placed edge to edge. (4)