Applikationsspecifika Integrerade kretsar

Tentamen

TSTE81

för Y4, D4 och TE

Tid:	Onsdag 19 Mars 1997 kl. 14.00 - 18.00
Plats:	FOA1, FOA2, FOA5
Ansvarig lärare:	Kent Palmkvist, 281347
Hjälpmedel:	Räknedosa, Formelsamling i Aktiva och Tidsdiskreta filter, Formelsamling i kretsteori samt allmänna tabellverk.
Anvisningar:	För godkänd tentamen fordras ca 30 poäng
Visning:	Torsdag 3 April 1997 kl. 13.00-14.00 (Lars Wanhammars tjänsterum)
Lösningar:	Anslås på Systemtekniks anslagstavla i labkorridoren
Betygslista:	Anslås senast 1997-04-03 på anslagstavlan i labkorridoren

1. a) What is an heuristic algorithm? (2)

   b) What is the difference between multiprocessor and multicomputer systems? Describe the principal architectures. (2)

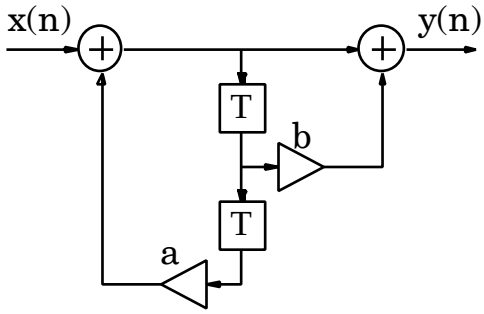
   c) Name two different redundant number systems. (2)

   d) Describe four approaches to partitioning of a system into a set of subsystems. (4)

2. The filter below is to be implemented with a sample period of 5 time units. The multiplication *a* requires 6 time units, multiplication *b* requires 4 time units, and each addition requires 1 time unit.

   a) Draw the precedence graph of the algorithm. (6)

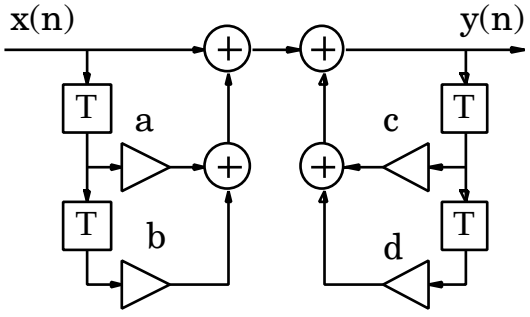
   b) Schedule the operations in order to reach the required sample period. (10)



3. The filter below is to be implemented using homogenous, non-preemptive processing elements. Operation *a* requires 4 time units, *b* requires 5 time units, *c* requires 3 time units, *d* requires 7 time units, and each addition requires 1 time unit.

   a) Determine the minimal sample period. (4)

   b) Determine a lower limit on the number of required processing elements if the sample period is 6 time units. (4)



4. The equations below describes an algorithm that is to be implemented using distributed arithmetic.

$$y(n) = 0.101_2x(n) - 0.11_2v_2(n)$$
$$v_1(n+1) = v_2(n)$$
$$v_2(n+1) = 0.1101_2x(n) + 0.111_2v_1(n)$$

a) Draw the structure of the complete filter using distributed arithmetic units, shift registers etc. as building blocks. (2)

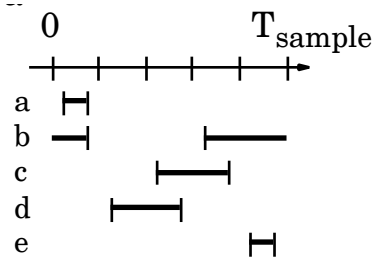
b) Determine the contents of the ROM(s). (6)

c) The size of the ROM(s) are reduced by utilizing the subtract/add signal in the shift accumulator. Determine the new contents of the ROM(s). (4)

3. The variables in the lifetime diagram below is to be stored using a RAM. Assign memory cells using

a) Clique partitioning (6)

b) Left edge algorithm (6)



5. A multiplication by the constant factor 45_{10} is to be implemented using bitserial arithmetic. The input is a bit-serial bitstream with least significant bit first. Only two adders are allowed. (Hint: 45=5*9). (6)

6. Introduce shimming delays in the structure below which is to be implemented using bit-serial arithmetic. The multiplication has a latency of 3 clock cycles, and the additions one clock cycle. (6)