ASIC for DSP

TEN1 TSTE87

Time:	Thursday January 15 2009, 08:00–12:00
Location:	U14
Responsible teacher:	Oscar Gustafsson, ISY, 013-28 40 59, 0768-02 77 97 Will visit the exam around 09:30 and 11:30
Allowed aid:	Calculator
Instructions:	The exam consists of four pages with a total of seven problems For passing 30 points are required The maximum score is 70 points Total points on first question = min {10, (oral exam points + first question points)} That is, you are free to solve an arbitrary number of the subproblems of question 1. Total points on the first question will never exceed 10.
Solutions:	Corridor C between B25 and B27.
Grades:	Posted at latest January 29 2009 as above.
Display:	Time and place will be posted along with the grades.

1. Please write the number of points obtained from the oral exam if you recall. (This will of course be double checked after deanonymization.)

   a) What is the difference between an iterative and a block processing DSP algorithm? (2)

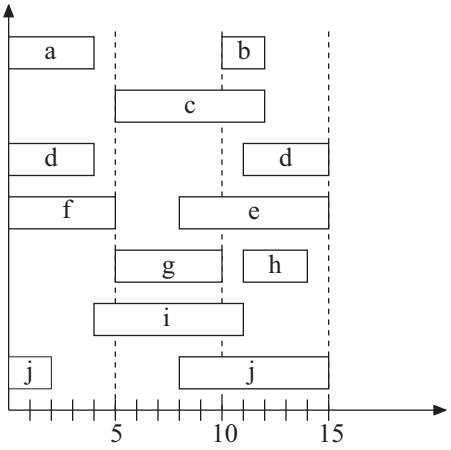
   b) What is the difference between a constructive and an iterative algorithm? (2)

   c) What is a redundant number system? Name two different redundant number systems. (2)

   d) Quantization can be performed in several different ways. Describe the operation of truncation, rounding, and magnitude truncation. (2)

   e) Describe two features of DSP processors that are especially suitable when implementing DSP algorithms. (2)

2. The lifetime diagram for a number of memory variables (a–j) is shown below. These should be implemented using a shared memory architecture where memories are of single wordlength and have one read port and one write port. Reading and writing can be done concurrently.



   a) Partition the memory variables between a minimal number of memories. (6)

   b) For each memory, assign memory variables to a minimal number of memory cells. (6)

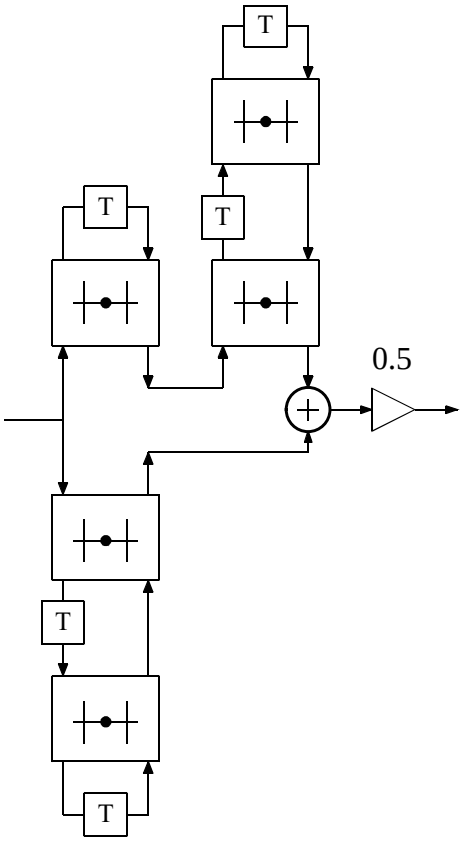
3. The following sum of product should be implemented using distributed arithmetic.

$$y = -\frac{7}{16}a + \frac{71}{256}b - \frac{19}{32}c + \frac{53}{64}d$$

   a) Determine the ROM contents. Use a suitable binary representation. (4)

   b) Determine the latency of the computation. (2)

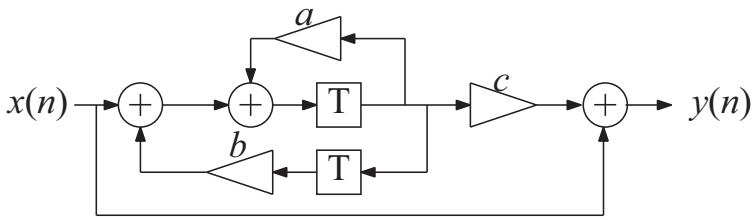
4. A decimation filter with a decimation factor of six will be implemented using Lattice Wave Digital Filters based on Richards' structures as illustrated by the fifth-order filter below.



The decimation will be performed in two stages, either as decimation by three followed by decimation by two or decimation by two followed by decimation by three. The required filter orders for the different cases are shown in the table below. Determine the required number of adaptors in a shared memory architecture for the different configurations assuming that the input sample rate is 100 MHz and that the execution time of an adaptor is 5 ns. Assume that you can **NOT** utilize polyphase decomposition and that the final addition and multiplication by 0.5 corresponds to one adaptor operation. (8)

Decimation factor 1	Decimation factor 2	Filter order 1	Filter order 2
3	2	5	5
2	3	3	7

5. The filter below is to be implemented using a shared memory architecture. The processing elements are homogenous and non-preemptive. The latency is four time units for the multipliers and three time unit for the adders. The execution time is two time units for the processing elements.



a) Determine the minimal sample period T_{min}. (2)

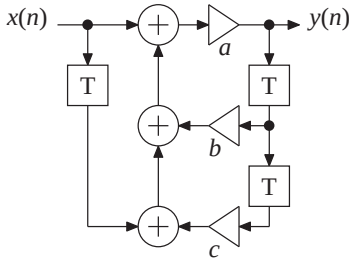
b) Determine the time of the critical path T_{cp}. (2)

c) Draw the signal-flow graph in precedence form. (6)

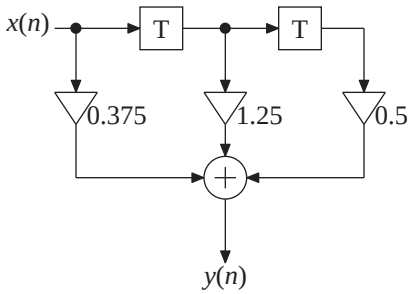
d) Schedule the algorithm so that $T_{sample} = T_{min}$. (8)

e) What is the smallest sample period obtainable if only one processing element is used? (2)

6. Apply arithmetic transformations to reduce the critical loop in the filter below to one addition and one multiplication. The total number of additions and multiplications should not be increased. (6)



7. The FIR filter below is to be implemented using isomorphic mapping to bit-serial processing elements. The data wordlength is 13 bits. Assume model 1, i.e., one pipeline register after each operation, for high clock rate.



a) Draw a fully specified signal flow graph. (2)

b) Introduce shimming delays. (6)