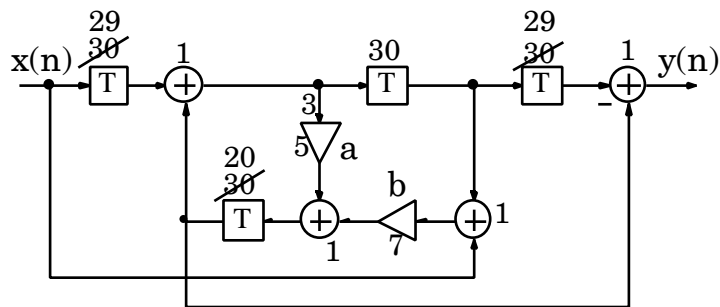
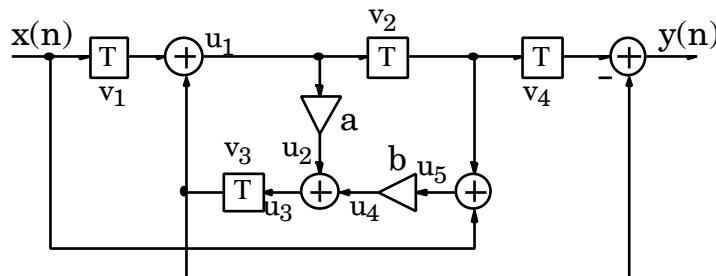


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1. a) The size of a distributed arithmetic unit grows asymptotically by 2^n .
 - b) Booths multiplier requires half the number of clock cycles compared to an ordinary shift-accumulator based multiplier.
 - c) Sign-magnitude truncation truncates the magnitude, even if the input is negative. Positive values are truncated, negative values are truncated and a least significant bit is added.
 - d) Preemptive processing elements can be interrupted in the middle of an operation, and that operation then restarted on another processing element. Non-preemptive processing elements cannot be interrupted in the middle of an operation.
 - e) Standard DSP solutions can be tested directly, while ASICs must be manufactured which takes in the range of weeks to months. This makes it more costly both in terms of money and time to correct a design error.
2. $150/5=30$ clock cycles/samples. Replace delay elements by 30 flip-flops, and start propagating them out in the circuit.



3. a) $T_{\min} = \max \{ (T_a + T_{\text{add}} + T_{\text{add}}) / 1, (T_b + T_{\text{add}} + T_{\text{add}} + T_{\text{add}}) / 2 \} = \max (7, 5) = 7$ clock cycles.
- b) Minimal resources = total computation time / available time. Homogenous PE:s => only one type of processing elements. $N = (4 * 1 + 7 + 5) / 7 = 2.3$. At least 3 processing elements are required.
- c) Name nodes:



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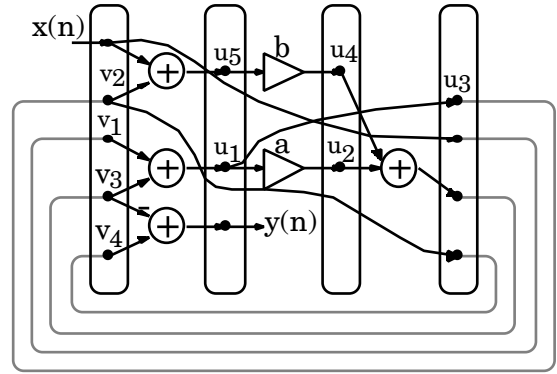
Node sets:

$$N_0 = \{ x(n), v_1(n), v_2(n), v_3(n), v_4(n) \}$$

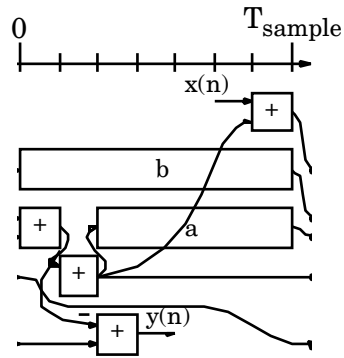
$$N_1 = \{ u_1, u_5, y(n) \}$$

$$N_2 = \{ u_2, u_4 \}$$

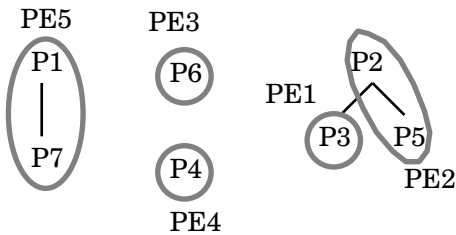
$$N_3 = \{ u_3 \}$$



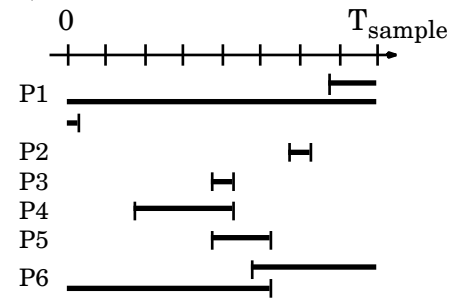
d)



4. a)

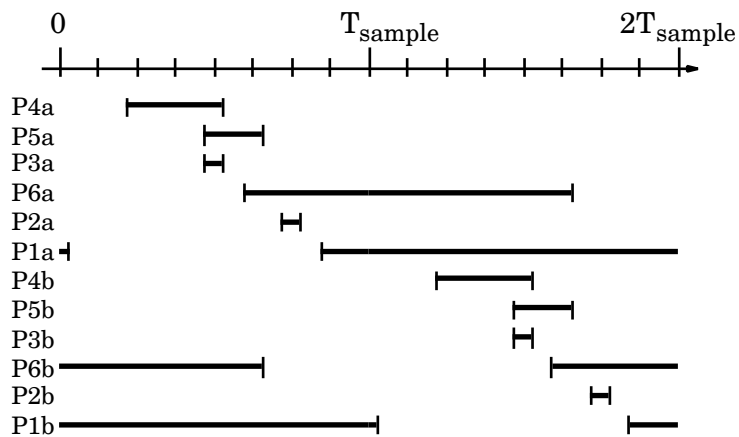


b)



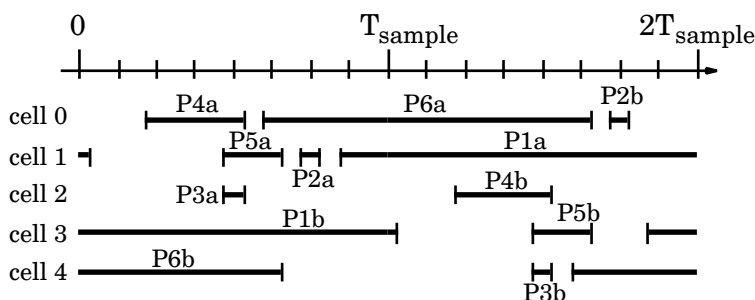
c) Variables has lifetimes longer than one sample period! => Allocate and assign for two sample periods!

1) Sort variables after starting time, if equal select longest first.

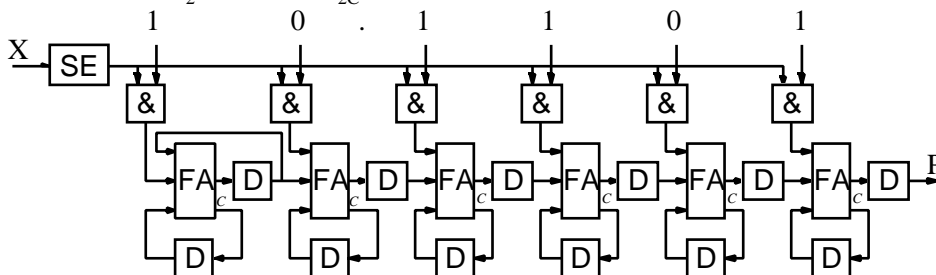


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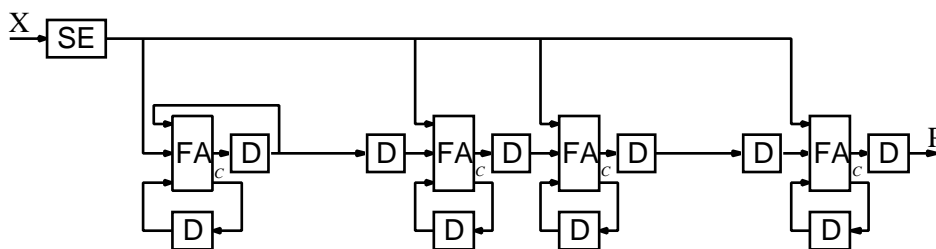
2) Allocate and assign starting from list of sorted lifetimes, until all variables assigned.



5. a) $-1.1875 = -1.0011_2 = 10.1101_{2c}$



b)



c) Latency = number of fractional bits + 1 = 4 + 1 = 5 clock cycles. If the last flip-flop is removed the latency is reduced to 4.

d) Throughput = number of clock cycles between starts of calculations. The multiplication generates $15 + 4 + 1 = 20$ bits out, where 4 bits are of lower significance than the least significant bit in the input, and 1 bit is of a higher significance than the most significant bit. One extra clock cycle may also be needed to reset the multiplier between operations.

e) $-1.1875 = -1 - 1/4 + 1/16 = -(1 + 1/4) + 1/16$

