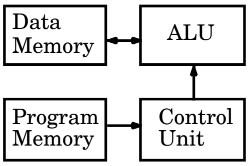
Tentalösningar ASIC (TSTE81) 970507

1. a) To find out the exact value requires a complete addition/subtraction of each bit => a Wd symbol word requires Wd additions/subtractions. The sign is however available as the sign of the most significant non-zero digit.

   b) No. Isomorphic mapping does not allow time-sharing of processing elements between different operations.

   c)



   d) Delay increases

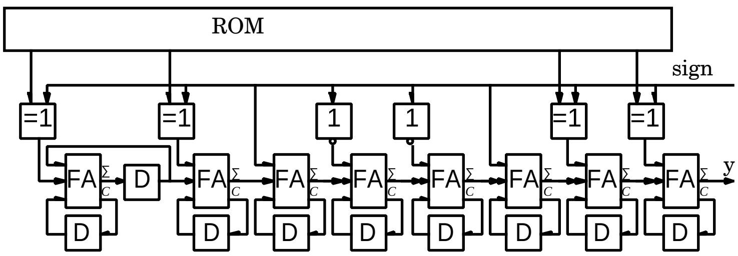
   e) Standard cell, sea of gates

2. a) Wf + 1 = 5 +1 = 6 clock cycles.

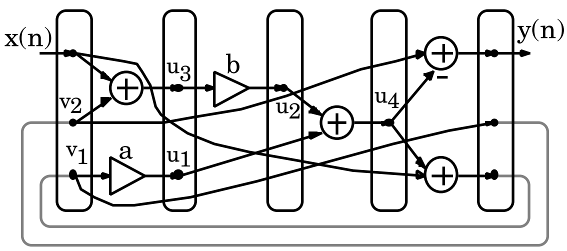
   b) Must process Wc+Wd – 1 bits. 2 guard bits should also be included in Wd. Assume only fractional coefficients => 12 + 5 = 17 clock cycles.

3. a) Removed from the exam due to incorrect problem definition. Should have stated "N word ROM uses 0.005*N mm^2".

   b)



4. a)

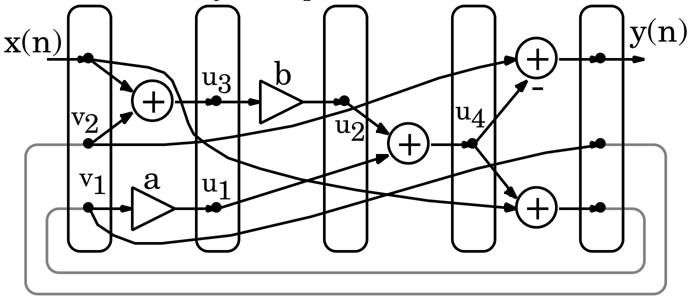


   b)

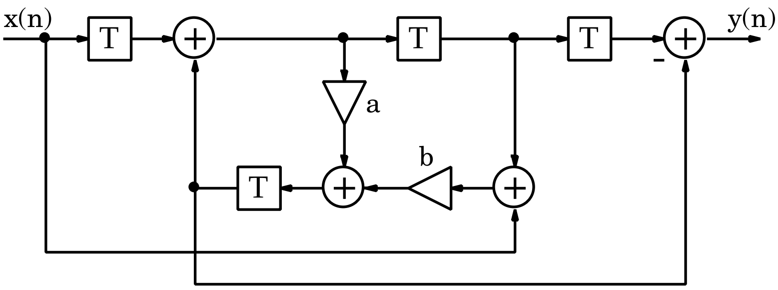
u3 := x(n) + v2
u1 := a v1
----
u2 := b u3
----
u4 := u2 + u1
----
y(n) := v2 – u4
----
v2(n+1) := v1
----
v1(n+1) := u4 + x(n)

u4 := b u3 + a v1
----
y(n) := v2 - u4
----
v2(n+1) := v1
----
v1(n+1) := u4 + x(n)

c) ALAP = As Late As Possible. Only multiplication a can be moved.



d)

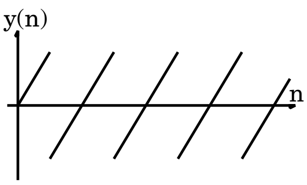


5. a) Divide the multi-input addition into an addition tree => $_2\log(n)$ adders depth.

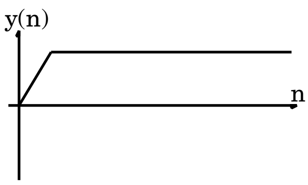
   $T_{min} = \max \{ T_{add}/1, (3T_{mult} + (2+{}_2\log(N))T_{add}) / 1\} = 3T_{mult} + (2 + {}_2\log(n))\ T_{add} = (3*4+(2*{}_2\log(n))*2)*50$ µs.

   b) Nonhomogenuous PE => separate multiplier and adder PEs. T_{sample} = 40 clock cycles.
   Adders: $(4 + 3 + 1) * 2 / 40 \leq 1$
   Multipliers: $(2*4 + 1) * 4 / 40 \leq 1$

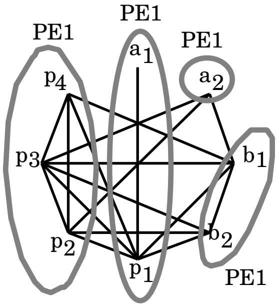
6. a)



b)



7. a)



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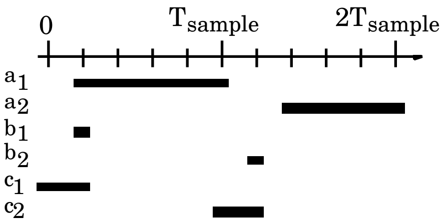
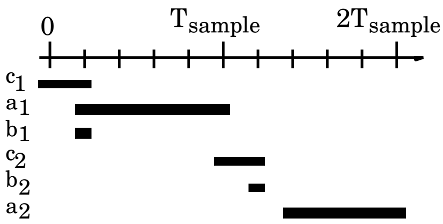
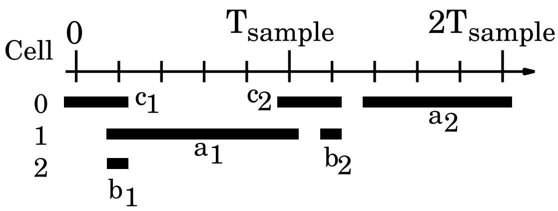
b)



c) 1: Sort





2: Assign