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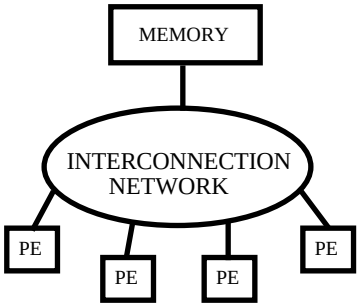
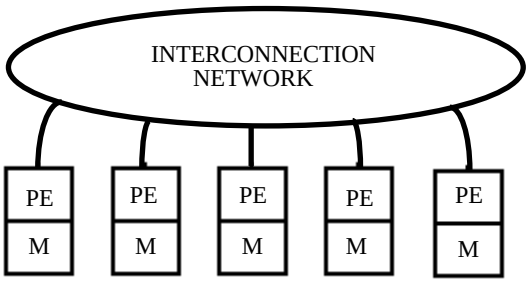
1. a) An heuristic algorithm finds solutions to a problem that are usually good enough using a computational complexity which is less than the best optimal solution algorithm.

   b) Multiprocessor:



   Multicomputer:



   c) Sign digit code, residue number systems

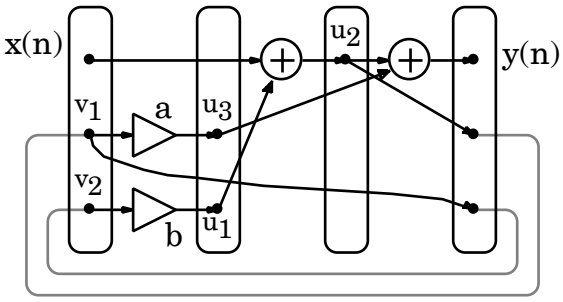
   d) Top down: The whole system is successively partioned into a hierarchy of subsystems.

   Bottom up: Successively assembling well-known building blocks into more complex blocks until the whole system is realized.

   Edge in: Partition the system into parts, starting from tine inputs and outputs and working inwards.

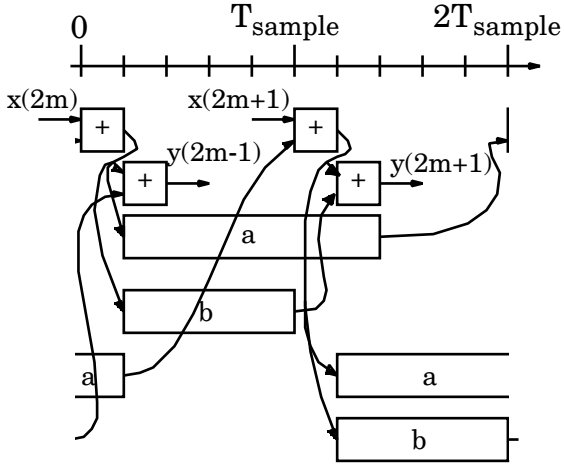
   Meet in the middle: The specification synthesis process is done top-down, but the actual design of the building blocks is performed in a bottom-up fashion.

2. a)



Tentalösningar ASIC (TSTE81) 970319

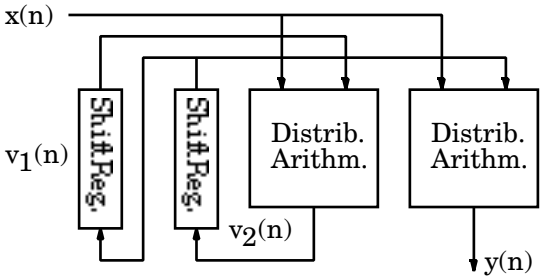
b) Operation time longer than sample period => Schedule period = 2 sample periods



3. a) Tmin = max { (3 + 1 + 1)/1, (7 + 1 + 1)/2 } = 5 time units.

   b) Homogenous => only one type of PE. Total computational load: 4 + 5 + 3 + 7 + 4 * 1 = 23 time units of work. Sample period = 6 time units => 23 / 6 = 3.8 ≤ 4. The lower limit is 4 processing elements.

4. a)



   b) Increase number reanges as needed.

x	v_1	ROM v_2
0	0	00.0000
0	1	00.1110
1	0	00.1101
1	1	01.1011

x	v2	ROM y
0	0	0.000
0	1	1.010
1	0	0.101
1	1	1.111

   c) Control add/sub using x.

   u_1 = x v1

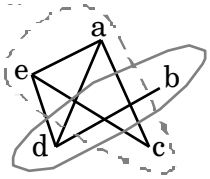
   u_2 = x v_2

u_1	ROM v_2
0	10.0101 (-0.1101 - 0.1110)
1	00.0001 (-0.1101 + 0.1110)

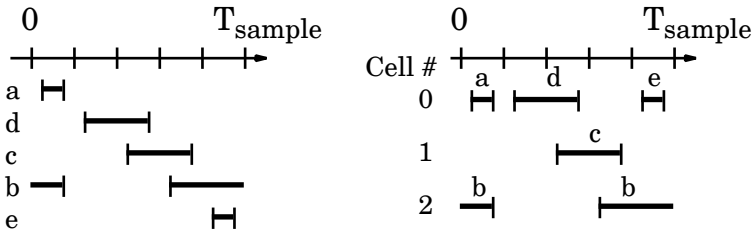
u_2	ROM y
0	00.001 (-0.101 - 1.010)
1	10.101 (-0.101 + 1.010)

Tentalösningar ASIC (TSTE81) 970319

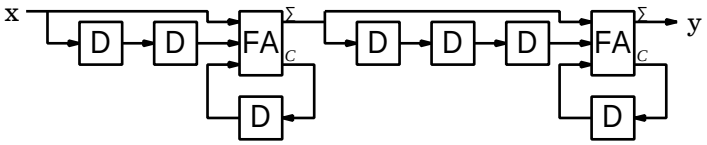
3. (7) a) Draw a connectivity graph, find as few cliques as possible => 2 cells are required.



b) Sort and assign => total of 3 cells required.



5. 45 = 5 * 9 = (4 + 1) * (8 + 1).



6. Total latency from input to output is 5 clock cycles.