Preliminary solutions to exam in TSTE 87 ASIC for DSP 2008-05-31

1. a) With saturation: The result is the maximum representable value.
Without saturation: The result "wraps" to become negative.
(An image is a good way of showing it, see the book.)

   b) $\frac{N}{2}\log_2 N$

   c) In a redundant number system a number may have more than one possible representation. Examples: Signed-Digit, Carry-Save
$001_{SD} = 01\bar{1}_{SD} = 1\bar{1}\bar{1}_{SD}$
$01_S\ 00_C = 00_S\ 01_C$

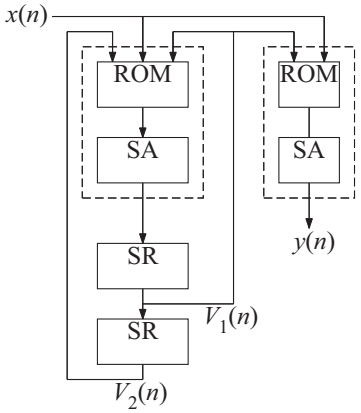
   d) Poles may be placed outside the unit circle for recursive algorithms
Overflow
Data quantization (non-linear operation)

   e) Carry lookahead, carry select, conditional sum, parallel prefix. (Carry-save is not really a good answer, but OK because of the book)

2. a) State-space representation

$$\begin{bmatrix} v_1(n+1) \\ v_2(n+1) \\ y(n) \end{bmatrix} = \begin{bmatrix} a & b & 1 \\ 1 & 0 & 0 \\ c & 0 & 1 \end{bmatrix} \begin{bmatrix} v_1(n) \\ v_2(n) \\ x(n) \end{bmatrix}$$

Architecture



b)

$v_1(n)$	$v_2(n)$	$x(n)$	Content	Rational	Binary (two's complement)
0	0	0	0	0	00.0000
0	0	1	1	1	01.0000
0	1	0	b	11/16	00.1011
0	1	1	1+b	27/16	01.1011
1	0	0	a	–3/8	11.1010
1	0	1	1+a	5/8	00.1010
1	1	0	a+b	5/16	00.0101
1	1	1	1+a+b	21/16	01.0101

$v_1(n)$	$x(n)$	Content	Rational	Binary (two's complement)
0	0	0	0	00.000
0	1	1	1	01.000
1	0	c	–3/8	11.101
1	1	1+c	5/8	00.101

c) DA determining $v_1(n+1)$: 4 clock cycles

DA determining $y(n)$: 3clock cycles

d) SR after DA determining $v_1(n+1)$: 21 D flip-flops

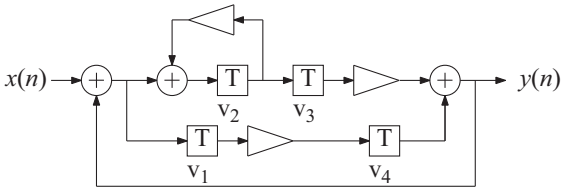
SR for storing $v_2(n+1)$: 25 D flip-flops

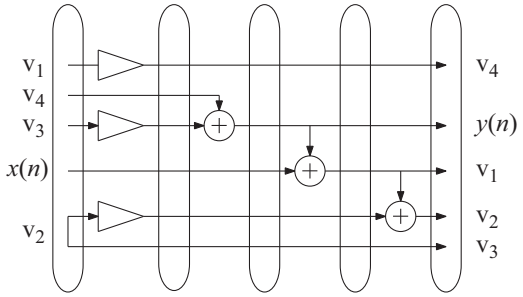
SR after DA determining $y(n)$: 22 D flip-flops (required only for synchronized inputs and outputs)

3. a) $T_{min} = \max\left\{\frac{T_{mult} + T_{add}}{1}, \frac{T_{mult} + 3T_{add}}{2}\right\} = 4$ t.u.

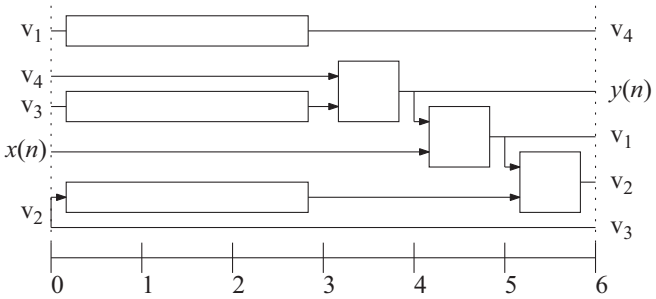
b) $T_{cp} = T_{mult} + 3T_{add} = 6$ t.u.

c) Introduce naming for (at least) the delay elements

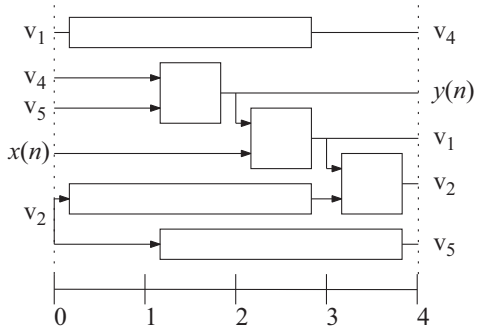




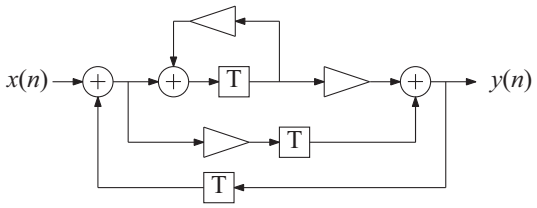
d) Initial schedule



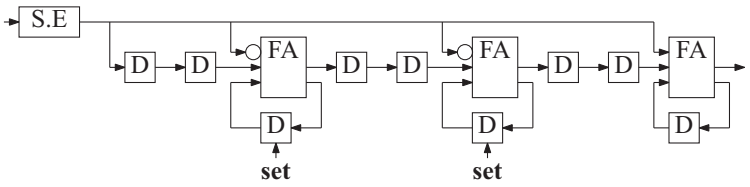
Reschedule (note the critical loop through V_2)



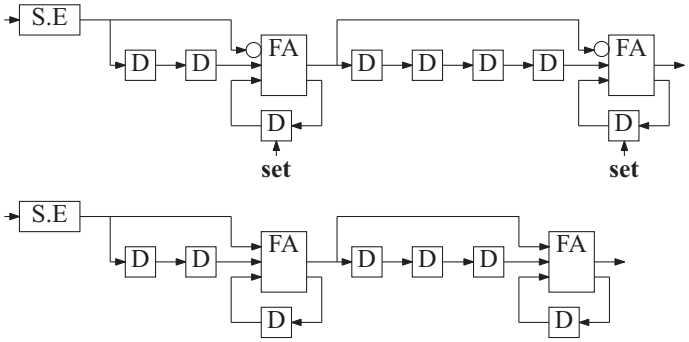
e)



4. a) $45/64 = 0.101101_{2C} = 1.0\bar{1}0\bar{1}01_{CSD}$

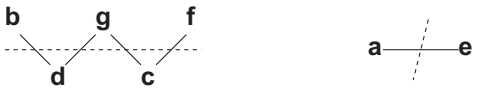


b)



c) 6 clock cycles for both cases (the number of fractional bits of the coefficient)

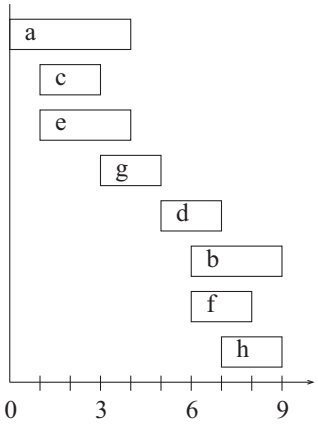
5. a) Construct exclusion graph based on concurrent read and write times. Variables named as the process that produced it.



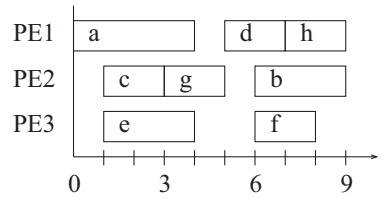
This gives that {b, f, g} should be placed in one memory with either a or e and that {c, d} should be placed in another memory with the remaining of a and e.

b) We here select to use the left-edge algorithm.

Sort according to start time



Perform allocation and assignment



c) $N_{PE} = \left\lceil \frac{\sum T_{exe}}{T_{schedule}} \right\rceil = \left\lceil \frac{20}{9} \right\rceil = 3$